

POWER ANALYSIS OF VLSI INTERCONNECT WITH RLC TREE MODELS AND MODEL REDUCTION

YOUNGSOO SHIN and JUNGHYUP LEE

*Department of Electrical Engineering,
Korea Advanced Institute of Science and Technology (KAIST),
Daejeon 305-701, Republic of Korea*

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The lumped capacitance model, which ignores the existence of wire resistance, has been traditionally used to estimate the charging and discharging power consumption of CMOS circuits. We show that this model is not correct by pointing out that MOSFETs consume only part of the energy supplied by the source. During this study, it was revealed that about 20% of the power is consumed in the wire resistance of the buffered global interconnect, when the interconnect is modeled with RC tree networks. The percentage goes up to 30 when RLC model is used indicating the importance of inductance in interconnect model for power estimation. For RLC networks, we propose a compact yet very accurate power estimation method based on a model reduction technique.

Keywords: Low power; interconnect; model reduction; CMOS.

1. Introduction

As the scale of process technologies steadily shrinks and the size of design increases, interconnects have an increasing impact on the area, delay, and power consumption of circuits. Reduction in scale causes a continual increase in interconnect delays, although, of course, overall circuit performance continues to increase. Traditionally, the effect of the interconnect on power consumption has been attributed to its capacitive component since the energy supplied by the source, which is then dissipated by MOSFETs during the charging and discharging processes, is proportional to the total capacitances. However, the resistive component also plays a role, especially in global interconnect systems, where large buffers drive long global interconnects, frequently in the order of mm.

Consider cascaded inverters, as shown in Fig. 1(a). The load seen by a driver is usually modeled as a lumped capacitance, as shown in Fig. 1(b), where C_g denotes the gate capacitance of a receiver. The lumped capacitance model has been traditionally used to estimate the charging and discharging power consumption of CMOS circuits, which constitutes a dominant factor in typical CMOS circuits. During the

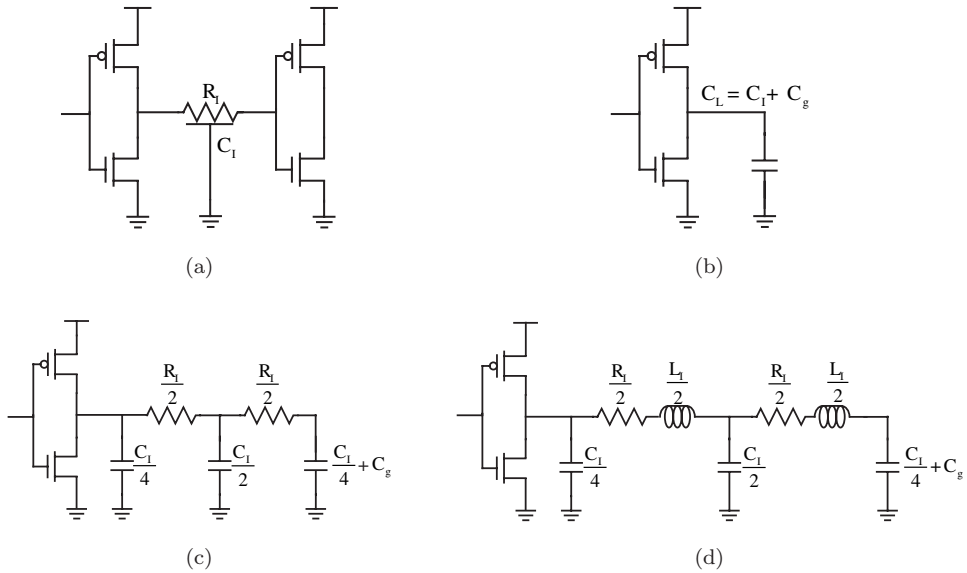


Fig. 1. (a) Two cascaded inverters, (b) lumped capacitance model for power estimation, (c) RC tree model for an interconnect, and (d) RLC tree model for an interconnect.

rising transition of the output, the total energy of $C_L V_{DD}^2$ is delivered by the source, the half is stored on C_L and the other half is dissipated by pMOSFET. The energy stored in the capacitor, $1/2 C_L V_{DD}^2$, is then dissipated by nMOSFET during the falling transition. Thus, the energy of $C_L V_{DD}^2$ is *entirely* dissipated by MOSFETs. The basic assumption of this model is that the interconnect resistance, denoted as R_I in Fig. 1(a), is negligible compared to the on-resistance of MOSFETs. This is generally true in local interconnects, where small MOSFETs (which therefore have large on-resistance) are connected by short wires that have low wire resistance.

However, the situation is different in global interconnect systems, where large MOSFETs (which therefore have small on-resistance) drive long global interconnects with large wire resistance. This is very common in System-on-a-Chip (SoC) style integration, where many bus interconnects are implemented through long global wires. Another example is a global clock,¹ which is constructed through huge clock buffers to simplify clock networks. The implication of this situation is that the traditional model for power analysis, such as the one shown in Fig. 1(b), is not valid for an interconnect system where wire resistance is significant.

If the interconnect is modeled as RC tree networks, such as the one shown in Fig. 1(c), the part of the energy supplied by the source is dissipated by wire resistances, during both the charging and discharging periods. We show in this paper that about 20% of the power is consumed in the wire resistance of the optimally buffered global interconnect system. We also show that this percentage goes up to 30 when an RLC model, such as the one shown in Fig. 1(d), is used, indicating

the importance of inductance in the interconnect model for power estimation. This is important, since, the inductance effects are particularly significant for global interconnect lines, such as those in clock distribution networks, signal buses, and power grids, based on longer metal interconnects and higher frequency operation.²

For VLSI interconnects with RLC tree models, we propose a compact yet very accurate power estimation method based on the model reduction technique. The separate evaluation of the driver and the interconnect contribution is very useful to understand the sources of energy dissipation, as well as to analyze the local increase in the temperature, which in turn degrades the reliability.

The remainder of the paper is organized as follows. In the next section, we discuss a buffered interconnect and address the power distribution over the technology nodes. In Sec. 3, a method of power distribution analysis based on a reduced-order model is introduced. In Sec. 4, we present results of experiments for several examples and in Sec. 5 we draw conclusions.

2. Power Consumption of a Buffered Interconnect

We consider a buffered global interconnect, as shown in Fig. 2(a), where interconnects are modeled as distributed RC networks. We especially try to build an *optimally buffered interconnect system*, where the buffer size and the number of buffers for a given length of an interconnect are determined in such a way that the delay is minimized. If an interconnect of length L is divided into k sections and $k + 1$ buffers are inserted, the total delay measured from the input of the first buffer to the output of the last buffer is given by³

$$\tau = k [p_1 R_i C_i + p_2 (R_t C_L + R_t C_i + R_i C_L)], \tag{1}$$

where R_i and C_i represent the resistance and capacitance of the wire of one section length, respectively, and R_t and C_L correspond to the on-resistance of the driver transistor and the input capacitance of the transistors that form the load,

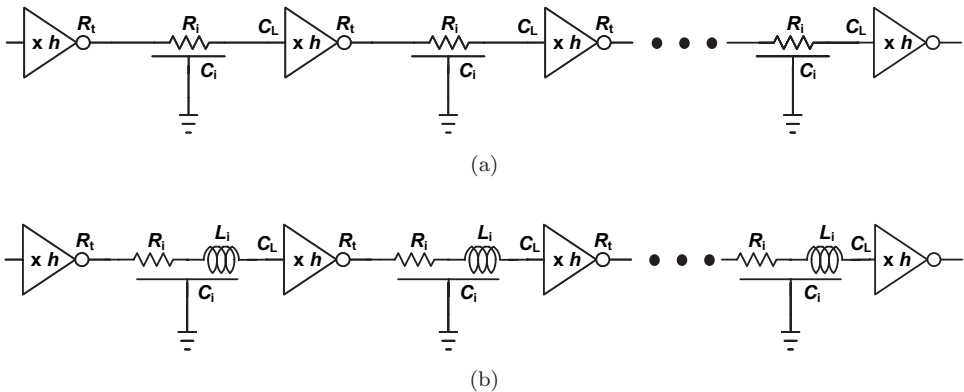


Fig. 2. Buffered global interconnects: (a) Distributed RC model and (b) distributed RLC model.

respectively. The constants p_1 and p_2 depend on the delay model and are equal to 0.377 and 0.693, respectively, when 50% delays are calculated, which we consider in this paper. The on-resistance of a minimum size MOS transistor, which we denote as r_t , can be obtained by³

$$r_t = \int_{V_1}^{V_2} \frac{dV}{I}, \quad (2)$$

where I is a function of V as defined by the $I_D - V_{DS}$ curve with $V_{GS} = V_{DD}$, and $V_1 = V_{DD}$ and $V_2 = V_{DD}/2$ in case of an nMOSFET. We can form a similar equation to (1) in terms of the resistance and capacitance of the wire of unit length (r_i and c_i) and the input capacitance of the minimum size transistors that form the load, c_L :

$$\tau = k \left[p_1 \frac{r_i L}{k} \frac{c_i L}{k} + \frac{r_t}{h} h c_L + \frac{r_t c_i L}{h} + p_2 \frac{r_i L}{k} h c_L \right], \quad (3)$$

where h denotes the size of buffers. Note that, we drop the constant p_2 from the terms that include r_t , since the on-resistance of MOSFET as defined by Eq. (2) includes the multiplicative constants in itself. Setting $\partial\tau/\partial h$ and $\partial\tau/\partial k$ equal to zero, respectively, gives us the optimal buffer size, denoted by h_{opt} , and the optimal number of sections, denoted by k_{opt} :

$$h_{\text{opt}} = \frac{1}{\sqrt{p_2}} \sqrt{\frac{c_i r_t}{r_i c_L}}, \quad (4)$$

$$k_{\text{opt}} = L \sqrt{p_1} \sqrt{\frac{r_i c_i}{r_t c_L}}. \quad (5)$$

Dividing L by k_{opt} yields the optimum section length:

$$l_{\text{opt}} = \frac{1}{\sqrt{p_1}} \sqrt{\frac{r_t c_L}{r_i c_i}}. \quad (6)$$

We use parameters extrapolated from predictive technology model,⁴ which are summarized in Table 1. Table 2 shows h_{opt} and l_{opt} that are obtained from Eqs. (4) and (6) with parameters in Table 1. For each technology node, we configure one section of the buffered interconnect (two buffers of size h_{opt} connected by the wire of length l_{opt}). The interconnect is modeled by five sections of RC π -ladders, which can very closely approximate the distributed RC networks.⁵ We apply the step at the input of the first buffer and measure the power consumption of the buffers and

Table 1. Technology parameters (r_i , l_i and c_i are per mm).

Tech.(nm)	V_{DD} (V)	T_{ox} (Å)	r_t (kΩ)	c_L (fF)	r_i (Ω)	l_i (nH)	c_i (fF)
180	1.8	40	3.3	1.18	22	1.66	154
130	1.5	33	3.5	0.79	31	1.69	158
100	1.2	25	3.6	0.59	37	1.70	171
70	1.0	16	4.3	0.44	41	1.71	192

Table 2. Parameters of optimally buffered interconnect systems.

Tech. (nm)	h_{opt}	l_{opt} (mm)
180	169	1.76
130	182	1.23
100	203	0.94
70	259	0.80

Table 3. Percentage of power consumption in wires of an optimally buffered interconnect system.

Tech. (nm)	RC model	RLC model
180	0.23	0.30
130	0.21	0.29
100	0.21	0.30
70	0.20	0.29

that of the interconnect (sum of power consumption of five resistors in π -ladders) through a SPICE simulation. The result is shown in Table 3, which indicates that about 20% of the power is consumed in wire resistance, and the trend is highly consistent over the technology nodes. This confirms the fact that the traditional lumped capacitance model for the analysis of the charging and discharging power consumption of MOSFETs is not accurate.

We repeat the same experiment, but this time with the interconnect modeled with five sections of RLC π -ladders instead of RC. The result is again shown in Table 3. About 30% of the power is consumed in wire resistance. Since the energy supplied by the voltage source is the same in RC and RLC tree networks, this implies that including inductance components increases (decreases) the power consumption of wire resistance (MOSFETs). The experiment confirms that we need to take inductive (as well as resistive) components of an interconnect into account in order to accurately analyze the power consumption. Note that we report the power consumption of RLC networks based on parameters (h_{opt} and l_{opt}) derived from the optimally buffered RC interconnect system, although those derived from the RLC interconnect are different.⁶ Because, the power distribution with the same buffer size and the same section length allows us to compare RC and RLC networks and, therefore, the impact the inductance can have on the power distribution behavior.

3. Power Estimation of RLC Interconnects

Once the interconnect is modeled with RLC tree networks, the entire circuit can be simulated with SPICE to obtain the power consumption at each resistor branch; however this is very time consuming since practical circuits contain an extremely large number of passive components, especially when circuit components are extracted from the geometry of the layout. We instead rely on a model reduction,

which is a technique that takes a circuit and reduces it to a smaller representation consisting of the dominant poles from the original circuit.

An RLC circuit can be described by a second-order matrix differential equation:

$$\mathbf{T}\mathbf{j} + \mathbf{W}\dot{\mathbf{j}} + \mathbf{U}\ddot{\mathbf{j}} = \mathbf{b}, \tag{7}$$

where \mathbf{j} is an n -dimensional column vector consisting of branch currents and \mathbf{b} denotes the system's input. \mathbf{T} , \mathbf{W} , and \mathbf{U} are an $n \times n$ matrix. We apply the Laplace transform to (7) assuming zero initial conditions, which yields

$$\mathbf{T}\mathbf{J} + s\mathbf{W}\mathbf{J} + s^2\mathbf{U}\mathbf{J} = \mathbf{B}, \tag{8}$$

where \mathbf{J} and \mathbf{B} denote the Laplace transforms of \mathbf{j} and \mathbf{b} , respectively. If \mathbf{J} has a Taylor series expansion about $s = 0$ (i.e., Maclaurin series), then it can be described by

$$\mathbf{J} = \sum_{i=0}^{\infty} \mathbf{M}_i s^i. \tag{9}$$

Substituting (9) into (8) and equating like powers of s , we have

$$\mathbf{M}_0 = \mathbf{T}^{-1}\mathbf{B}_0, \tag{10}$$

$$\mathbf{M}_1 = -\mathbf{T}^{-1}\mathbf{W}\mathbf{M}_0, \tag{11}$$

$$\mathbf{M}_i = -\mathbf{T}^{-1}(\mathbf{W}\mathbf{M}_{i-1} + \mathbf{U}\mathbf{M}_{i-2}), \quad i \geq 2. \tag{12}$$

In a reduced-order model, especially one obtained by moment matching, $J(s)$ is approximated by the reduced-order system of a proper rational function of s having q -poles:

$$\hat{J}(s) = \frac{n_{q-1}s^{q-1} + n_{q-2}s^{q-2} + \dots + n_1s + n_0}{s^q + d_{q-1}s^{q-1} + \dots + d_1s + d_0}. \tag{13}$$

Since, there are $2q$ unknowns in the reduced-order system, Eq. (13) is forced to correspond to the first $2q$ terms of Eq. (9) by using Padé approximation, yielding the following equality:

$$\begin{aligned} & \frac{n_{q-1}s^{q-1} + n_{q-2}s^{q-2} + \dots + n_1s + n_0}{s^q + d_{q-1}s^{q-1} + \dots + d_1s + d_0} \\ & = m_0 + m_1 + \dots + m_{2q-1}s^{2q-1}. \end{aligned} \tag{14}$$

Multiplying both sides of Eq. (14) by the denominator of the left-hand side yields a set of equations that can be solved for $2q$ coefficients. After finding the roots of the denominator of the reduced-order model, Eq. (13) can be expressed as a partial fraction expansion form given by

$$\hat{J}(s) = \sum_{i=1}^q \frac{r_i}{s - p_i}, \tag{15}$$

where r_i is the residue of $\hat{J}(s)$ at the pole p_i . It is then straightforward to obtain the time-domain current $\hat{j}(t)$.

Once the current is available from Eq. (15), the approximate energy dissipated by R_i , denoted by \hat{E}_i , during time period $[t_1, t_2]$ is then given by

$$\hat{E}_i = R_i \int_{t_1}^{t_2} \hat{j}^2(t) dt. \quad (16)$$

If we are interested in the total energy dissipated by a specific resistor element during signal transition, we can choose to consider a semi-infinite interval of t , without loss of generality. We make t_1 the time origin and t_2 infinite time. Then $\hat{j}(t)$ will reach a steady state, provided that $\hat{j}(t)$ corresponds to the reduced-order model of an individual transition. This leads us to the improper integral

$$\hat{E}_i = R_i \int_0^{\infty} \hat{j}^2(t) dt. \quad (17)$$

The direct computation of improper integration is difficult, especially if there are multiple-order poles or if $\hat{j}(t)$ is expressed as a combination of functions other than exponentials. Fortunately, we can avoid this by relying on a general relation between improper integration in the time-domain and algebraic computation in the s -plane, as proposed in Ref. 7, which we repeat here for reference.

Theorem 1. *If the Laplace transform of a time-domain signal $h(t)$, denoted by $H(s)$, has q singularities in the left half of the s -plane, then*

$$\int_0^{\infty} h^2(t) dt = \sum_{i=1}^q \tilde{r}_i, \quad (18)$$

where \tilde{r}_i is a residue of $H(-s)H(s)$ at the singularity of $H(s)$.

Note that the only constraint imposed by the Theorem 1 is that the transfer function has singularities to the left of the s -plane, which is a typical situation because, we are mostly concerned with stable systems. In the case when all the singularities are simple poles, there is a less complicated relation expressed by the following theorem.

Theorem 2. *If the Laplace transform of a time-domain signal $h(t)$, denoted by $H(s)$, has q simple poles in the left half of s -plane, then*

$$\int_0^{\infty} h^2(t) dt = \sum_{i=1}^q r_i H(-p_i), \quad (19)$$

where r_i is a residue of $H(s)$ at the pole p_i of $H(s)$.

4. Experimental Results

We implemented a prototype tool written in C++ and based on the method presented in the previous section. Since, the accuracy and stability of the result depend on the accuracies of the poles and residues in the reduced-order model, the result

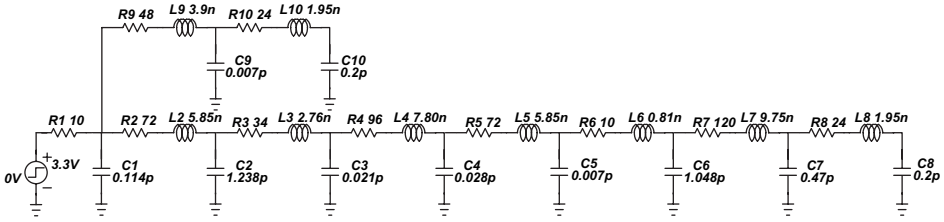


Fig. 3. An RLC tree example.

presented in this section could be improved using more advanced techniques than the moment matching-based one we used in the paper.

We constructed the first example based on the RC tree,⁸ which has widely varying time constants and, thus, is difficult to approximate. Since, the original circuit does not contain inductors, we include an inductor in a series with each resistor. The inductance is scaled with respect to the resistance of the resistor that is in series with it, i.e., $L_i = (R_i/r)l$, where r and l are the resistance and inductance of a global wire of unit length extrapolated from Ref. 4, respectively. The resulting RLC tree is shown in Fig. 3.

First, we compare the energy dissipation of each resistor in the RC and RLC trees through SPICE simulation. The results are tabularized in Table 4, where the energy dissipation is of the order of pJ. We can see that the total energy is the same in RC and RLC trees ($1/2 C V_{DD}^2$, where C is the sum of capacitances), as it must be. However, the energy *distribution* is significantly different. Energy dissipation of R1, which can be considered as the on-resistance of MOSFET, in the RLC tree, is reduced by 17.4% compared to the RC tree, which coincides with the observation in Sec. 2.

In Table 5, we study the accuracy of our estimation method by comparing the estimation result with SPICE simulation. We increase the number of poles for our approximation, and Table 5 shows, as an example, the results with two-, six-, and

Table 4. Comparison of the energy dissipation in RC and RLC networks.

Resistor	RC	RLC	Difference (%)
R1	2.53	2.09	-17.3
R2	9.01	8.28	-8.1
R3	0.90	1.03	15.0
R4	2.48	2.88	16.1
R5	1.80	2.10	16.8
R6	0.25	0.29	16.8
R7	0.44	0.57	30.7
R8	0.01	0.01	32.0
R9	0.51	0.61	19.5
R10	0.24	0.30	23.1
Total energy	18.16	18.16	

Table 5. Comparison of the energy dissipation through SPICE simulation and the proposed estimation method.

Resistor	SPICE	2-poles	6-poles	9-poles
R1	2.09	1.66	1.55	2.08
R2	8.28	7.41	8.28	8.28
R3	1.03	1.08	1.03	1.03
R4	2.88	3.02	2.88	2.88
R5	2.10	2.21	2.10	2.10
R6	0.29	0.30	0.29	0.29
R7	0.57	0.59	0.57	0.57
R8	0.01	0.01	0.01	0.01
R9	0.61	0.44	0.61	0.61
R10	0.30	0.20	0.30	0.29
Avg. error (%)		11.9	2.7	0.1
Max. error (%)		31.1	25.9	0.7

nine-pole approximations. For the example circuit, we need nine poles to obtain less than a 1% maximum error. However, practical circuits usually do not have these varying time constants. An approximation with two or three poles gives accurate result most of time, which is consistently observed with many examples.

The second example consists of randomly generated RLC tree networks. We vary the number of nodes from 100 to 500, randomly generate resistance, and scale

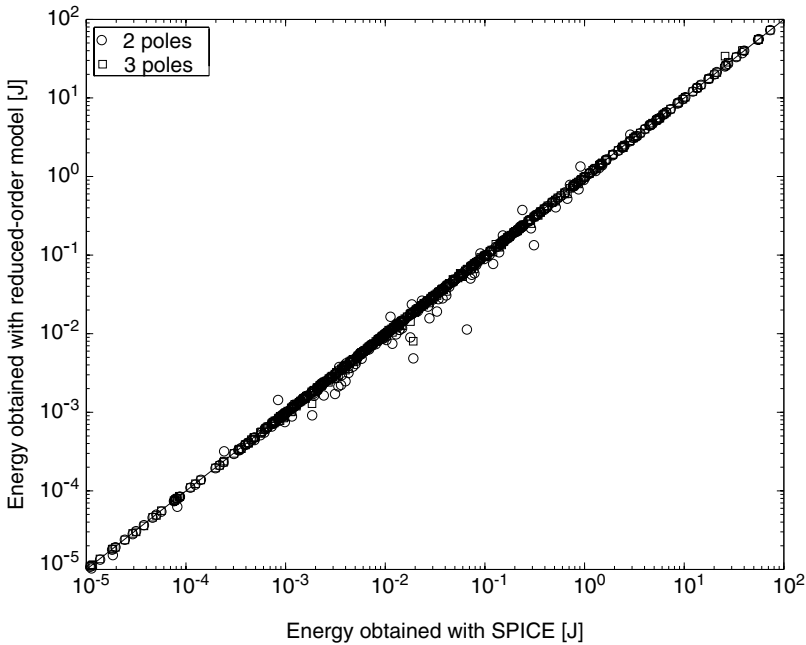


Fig. 4. Comparison of the energy distribution for randomly generated circuits having 500 nodes.

the inductance and capacitance accordingly, following the same procedure used in the first example. The resulting circuits are constructed in such a way that they also have widely varying time constants, although the number of poles needed to obtain a high accuracy level is less than in the first example. We compare the energy distribution obtained through SPICE simulation with that obtained by our method. The approximation with two or three poles yields accurate results for most cases, as can be seen in the example of a circuit having 500 nodes, as shown in Fig. 4.

5. Conclusion

We studied the interconnect power consumption based on current and future technology node parameters. The study shows that, for the case of optimally buffered global interconnect systems with RC tree models, about 20% of the power is changed to heat in interconnects, and this is in sharp contrast to the traditional CMOS power consumption model, where interconnect power consumption is neglected. The percentage goes up to 30 when the RLC model is used, which indicates the importance of inductance in high frequency deep submicron technology.

We describe a method for the power distribution analysis of an interconnect with RLC tree networks based on a reduced-order model. The separate evaluation of the driver and the interconnect contribution is very useful to understand the sources of energy dissipation, as well as to analyze the local increase in the temperature, which in turn degrades the reliability.

References

1. K. M. Carrig, N. T. Gargiulo, R. P. Gregor, D. R. Menard and H. E. Reindel, A new direction in ASIC high-performance clock methodology, *Proc. IEEE Custom Integrated Circuits Conf.* (May 1998), pp. 593–596.
2. A. Deutsch *et al.*, When are transmission-line effects important for on-chip interconnections?, *IEEE Trans. Microwave Theor. Tech.* **45** (1997) 1836–1846.
3. H. B. Bakoglu, *Circuits, Interconnects, and Packaging for VLSI* (Addison-Wesley, 1990).
4. Device Group at UC Berkeley, Berkeley predictive technology model, <http://www-device.eecs.berkeley.edu/ptm/>.
5. T. Sakurai, Approximation of wiring delay in MOSFET LSI, *IEEE J. Solid-State Circuits* **SC-18** (1983) 418–426.
6. Y. I. Ismail and E. G. Friedman, Effects of inductance on the propagation delay and repeater insertion in VLSI circuits, *IEEE Trans. VLSI Syst.* **8** (2000) 195–206.
7. Y. Shin and T. Sakurai, Power distribution analysis of VLSI interconnects using model order reduction, *IEEE Trans. Computer-Aided Design* **21** (2002) 739–745.
8. L. T. Pillage and R. A. Rohrer, Asymptotic waveform evaluation for timing analysis, *IEEE Trans. Computer-Aided Design* **9** (1990) 352–366.