Cell-Based Semicustom Design of Zigzag Power Gating Circuits

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Abstract

Zigzag power gating (ZPG) has been proposed to overcome the drawback of power gating in its long wakeup delay. However, the use of both NMOS and PMOS current switches in zigzag fashion makes power networks very complicated. This has limited the application of ZPG circuits only to custom design. This paper proposes cell-based semicustom design of ZPG circuits. A new power network architecture is proposed that allows unmodified conventional logic cells to be used. The circuit elements that supplement the cell-based ZPG design are then discussed. To optimize the physical design of ZPG circuits, two methods are proposed. The area is optimized by modulating the number of different types of circuit rows. The wirelength is optimized by selecting the sleep vector that leads to shorter wirelength between flip-flops and their fanin and fanout gates.

1. Introduction

Subthreshold leakage current grows exponentially with every process generation, due to the scaling down of threshold voltage. It has become a major portion of total power consumption, and, in many technologies, it contributes up to 50% of the overall power consumption [1].

Power gating [2] is one of the most effective technique to limit the subthreshold leakage. Power gating refers to gating, or cutting off, a circuit from its power supply rails during standby mode. Either PMOS or NMOS can be used as a gating device, where the former is referred to as a header while the latter as a footer. In case of a footer, once it is turned off, the virtual ground (V_{ssv}), where the footer has its drain and the circuit sinks its current, slowly goes up until it reaches a steady state potential, which is usually close to V_{dd}. This implies that all the nets internal to the circuit are charged up to V_{dd} irrespective of their logic states.

Thus, many of those nets, which were charged up during standby mode, start to be discharged together once footer is turned on. This leads to a large amount of current flowing into the footer, which, together with parasitic of power networks and a package, is a source of large wakeup delay of power gating. As an example, we take c7552, one of ISCAS benchmark circuits, which consists of 1713 gates after mapping it on to a commercial 180nm, 1.8V gate library. We connect a properly sized footer to the circuit to see its wakeup delay. Figure 1(a) shows the delay, which is the interval from turning on the footer to a point when V_{ssv} settles down to its steady state potential, which is close to V_{ss}. It takes about 2.68ns, which is large for this circuit of small size. We then combine the RLC model of a package [3] with our circuit, and simulate the whole circuit to see the realistic wakeup delay. From Figure 1(b), it is clear that the large amount of current flowing into the footer can induce

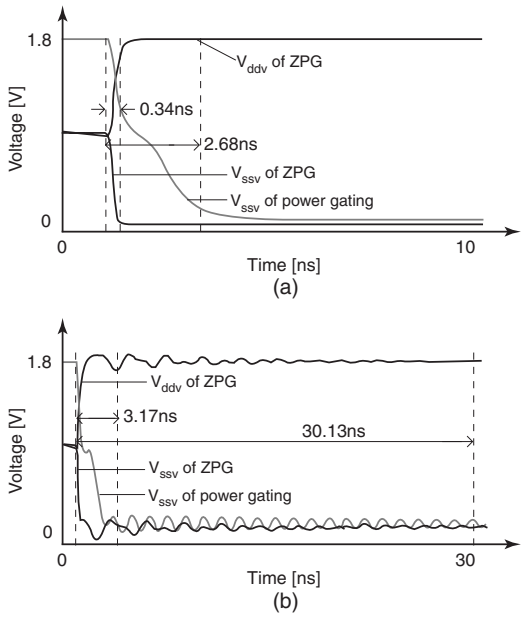

Figure 1. Wakeup delay of power gating and ZPG circuits (a) without and (b) with package model.

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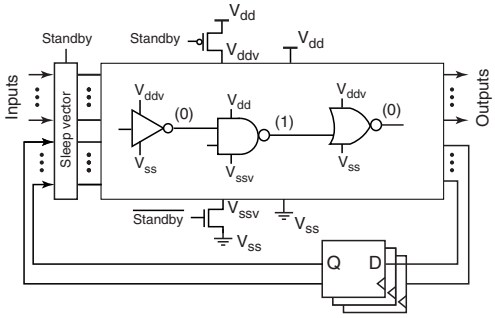

Figure 2. Zigzag power gating circuit.

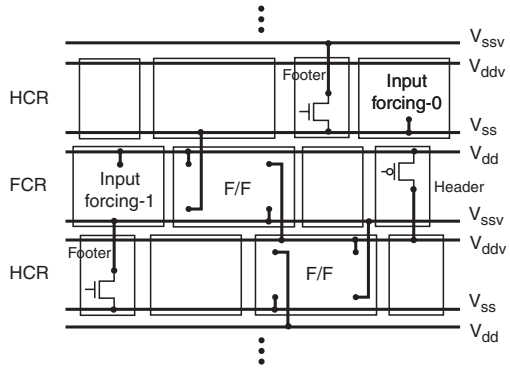

Figure 3. Power networks for zigzag power gating.

ground bounce, which in turn leads to substantial amount of time (30.13ns) for wakeup.

Zigzag power gating (ZPG) [4], [5], [6] can alleviate this drawback to power gating. Figure 2 shows the concept of ZPG. Before entering standby mode, an input vector, called *sleep vector*, is applied to the circuit (the block for sleep vector is transparent during active mode). For sequential circuit, part of the sleep vector corresponds to primary inputs, while the outputs of flip-flops are responsible for the remaining part. Since the sleep vector is pre-determined, the logic state of all the nets during standby mode are known a priori. For those gates whose outputs are logic high, we use a footer; the remaining gates are connected to a header. Once the footer and the header are turned off, their drain potentials slowly go up and go down respectively until they reach the steady state potentials. However, as opposed to power gating, all the nets keep their logic states[1]. Thus, there is no need to discharge the nets to restore their logic states when coming back to active mode. This is why, as shown in Figure 1, the wakeup delay of ZPG for the same example circuit is considerably shorter (0.34ns and 3.17ns without and with package model) than that of power gating.

On the other hand, the use of both footer and header in zigzag fashion has a drawback of complicated power networks. In particular, since ZPG has very diverse power requirements[2], we cannot use the conventional standard cells with conventional power networks having V_{dd} and V_{ss} rails. In fact, this is very crucial to the widespread use of ZPG circuits, because most modern VLSI design depends on cell-based top-down design methodology.

In this paper, we propose a *design methodology for cell-based ZPG circuits*. Specifically, a power network architecture is proposed that enables the use of conventional standard cell elements without any modification. We present the circuit elements that supplement the cell-based ZPG design in the proposed power network. These include flip-flops, input forcing circuits, and current switches. The placement is done in the fashion of interleaved circuit row, which is similar to the placement for dual V_{dd} circuits [7]. The proposed methodology is tested using benchmark circuits in terms of area and wirelength. In order to optimize the physical design, two methods are proposed. The first one tries to reduce the area by modulating the number of different types of circuit rows. The second method reduces the total wirelength by selecting the sleep vector that leads to shorter wires between flip-flops and their fanin and fanout gates.

The remainder of this paper is outlined as follows: in the next section, we describe our power network architecture. In Section 3, we present the circuit elements for ZPG design. The physical design optimization methods are also addressed. Experimental results are presented in Section 4, and we draw conclusions in Section 5.

2. Power Network Architecture

Figure 3 shows the proposed power network architecture. It has two types of circuit rows. The first type, which we call *header-connected circuit row* (HCR), has V_{ddv} and V_{ss}; the gates that are connected to a header are placed in HCRs. The second type, called *footer-connected circuit row* (FCR), has V_{dd} and V_{ssv}; it is a site for the gates that are connected to a footer. The VDD and GND terminals of gates are naturally connected to respective power rails. Therefore, we use the conventional standard cells without any modification, except that their placement is restricted to either type of circuit row. However, by using a feedthrough, we may use the same circuit row as a site for both types of gates [7] at the cost of customized placement.

Since we use unmodified conventional standard cells,

[1] As an example of the inverter in Figure 2, the NMOS remains turned-on even though the header, which is in series with the PMOS, is turned off.

[2] Some gates are connected to V_{ddv} and V_{ss}; some are connected to V_{dd} and V_{ssv}; flip-flops require all four power rails as will be explained in Section 3; header is connected to V_{dd} and V_{ddv}; and footer is connected to V_{ssv} and V_{ss}.

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where the body (or substrate) is tied to GND terminals[3], the body of gates in HCR is tied to V_{ss}, while those gates in FCR have their bodies tied to V_{ssv} (GND terminals of gates in FCR are connected to V_{ssv} rails). To avoid this electrical short between V_{ss} and V_{ssv}, the body contacts of all cells in FCR are removed after placement. This implies that the gates in FCR experience reverse body bias, because their bodies are biased to V_{ss}, while their GND terminals are tied to V_{ssv}, which is higher than V_{ss}. However, by properly sizing the footer [8], the delay increase from this reverse body bias can be made negligible. This negative effect from reverse body bias can be totally eliminated if triple-well process is available, since p-wells of each circuit row can be isolated each other.

Although the logic gates are restricted in their placement, it is important to be able to allow clocked elements, such as flip-flops, to be placed anywhere in the placement region. This is because flip-flops are often the leaves of clock tree network [9], and thus if their placement is restricted, the associated circuit elements in the clock tree such as buffers and clock splitters are restricted in their placement as well, which in turn makes clock design very difficult. To guarantee unrestricted placement and to provide all four power rails (will be explained in the next section), we re-design flip-flops such that they are connected to adjacent power rails through their ports instead of VDD and GND terminals as shown in Figure 3.

The footer cells are placed in HCRs due to the availability of V_{ss}. Their drains are connected to V_{ssv} in adjacent FCRs as shown in Figure 3. In the same way, the header cells are placed in FCRs and they draw V_{ddv} from adjacent HCRs. The design of footer and header cells themselves will be explained in the next section.

Input forcing circuit (refer to Figure 2) is a circuit that is located at each primary input to provide a sleep vector. The one that provides logic high is placed in FCRs; the one for logic low is placed in HCRs as shown in Figure 3. Their design will be discussed in the next section.

3. Physical Design of ZPG Circuits

In this section, we first present the circuit elements that supplement the cell-based ZPG design in the proposed power network. Since the placement is done in the fashion of interleaved circuit row, there is an overhead in terms of area and wirelength. Then, we propose two methods: one to reduce the area through modulating the number of HCRs and FCRs; another to reduce the wirelength via optimizing sleep vector.

[3]We assume that well or substrate contacts are present in each standard cell element.

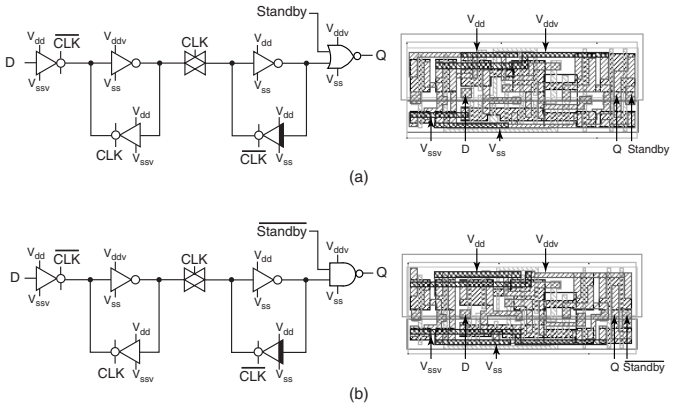

Figure 4. ZPG D flip-flops with (a) phase forcing low and (b) phase forcing high.

3.1. ZPG Cell Design

Figure 4 shows ZPG D flip-flops. The first flip-flop in Figure 4(a) is used where we want logic low in the sleep vector, which the NOR gate at the output is responsible for (note that the flip-flop outputs are part of sleep vector as shown in Figure 2). We use the second flip-flop when we want logic high in the sleep vector. Note that the two inverters in the second latch are directly connected to V_{dd} and V_{ss} instead of V_{ddv} or V_{ssv}, meaning that they are not power-gated. In this way, they are able to retain the state of the flip-flop during standby mode. In addition, the tri-state inverter in the second latch employs high V_{th} to reduce its subthreshold leakage while it does not affect the flip-flop delay. Note also that the NOR and NAND gate at the output are connected to header and footer, respectively, to reduce their subthreshold leakage.

The application of sleep vector determines the flip-flop input (D) during standby mode (refer to Figure 2), which implies that the logic states of three inverters at the front of the flip-flop are known. Therefore, those inverters are connected either to header or to footer depending on the flip-flop input during standby mode. Thus, we need four types of flip-flop in total depending on the flip-flop input and the enforced flip-flop output during standby. For example, the flip-flop in Figure 4(b) is used where the flip-flop input is logic low and we want logic high in the sleep vector. Since our flip-flops require all four power rails and we do not want to have any restrictions on their placement as discussed in the previous section, power rails are connected via ports instead of VDD and GND terminals, as shown in the layouts.

One last issue on ZPG flip-flop is n-well isolation. The proposed flip-flop has its n-well tied to V_{dd} due to the two inverters in the second latch, which are responsible for state retention. If it is placed in HCR, where the other cells have

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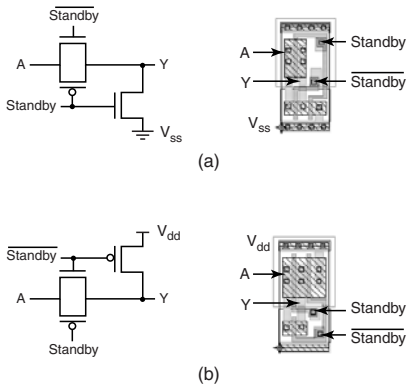

Figure 5. Input forcing circuits providing (a) logic low and (b) logic high.

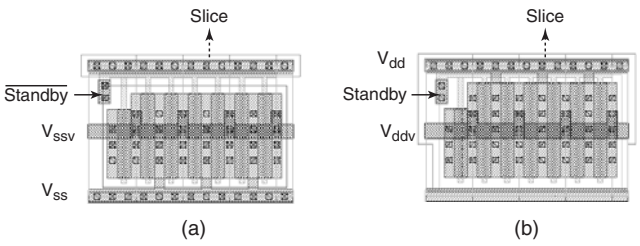

Figure 6. Layouts of (a) footer and (b) header.

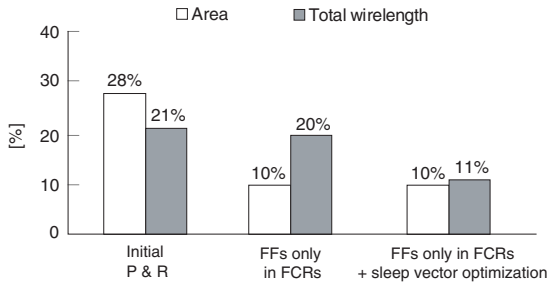

Figure 7. Overhead of area and total wirelength of s5378.

their bodies tied to V_{ddv} (refer to Figure 2), its n-well has to be isolated, which incurs area overhead. On the other hand, if it is placed in FCR, we can avoid the n-well isolation. This fact will be utilized in Section 3.2 to optimize area while we regulate the proportion of the number of FCRs and HCRs.

Figure 5 shows the circuits, which we call *input forcing circuits*. They are used at the primary inputs to provide the sleep vector. They are transparent during active mode (standby is low). In standby mode, the transmission gate de-couples the primary input from the circuit; NMOS and PMOS provide logic low and high respectively for the sleep vector. Note that the circuit in Figure 5(a), which enforces logic low is placed only in HCR because NMOS needs V_{ss} rails that are on HCR. The circuit in Figure 5(b) is placed in FCR.

Figure 6 shows the cell layouts of footer and header, respectively. A *slice* is a unit current switch; when slices are abutted together as shown in the figure, they form a large current switch (the cells on the left and right supplement the layouts). This allows us flexible placement strategy depending on power network requirement; we could have a large single footer and header (by abutting many slices together) in the center of the placement region, we could sprinkle small footers and headers over the placement region, and so on. The exact placement of footer and header is beyond the scope of this paper [10].

3.2. Physical Design Optimization

In order to see the feasibility of physical design with the proposed power network and ZPG cells in Section 3.1, we take s5378, one of ISCAS benchmark circuits. It consists of 2128 gates and 176 flip-flops after mapping it on to a commercial 180nm gate library. After converting the original circuit to ZPG circuit[4] followed by automatic placement and routing, the area is increased by 28% and the total wirelength by 21%, as shown in Figure 7. It is found out that the n-well isolation of flip-flops (the flip-flops placed in HCRs need their n-wells isolated from the other cells as was explained in Section 3.1) is a dominating factor of the area overhead.

In order to reduce the area overhead from n-well isolation, we first compute the area of cells placed in FCR and HCR, respectively, assuming that flip-flops will be placed only in FCRs. Then, we change the proportion of FCRs to HCRs from 1:1 to 3:1, i.e. one HCR after three FCRs. The design is then placed and routed again, while we restrict the placement of flip-flops to FCRs. The area overhead goes down to 10% as shown in Figure 7; the total wirelength remains almost the same. Note that flip-flops are not totally restricted in their placement in this example, because they are free to be placed in 75% of placement region. In general, the choice of flip-flop placement (unrestricted vs. only in FCRs) should be dependent on the proportion of total flip-flop area, which affects the number of FCRs in total circuit rows.

The profile of the total wirelength reveals that the wires between flip-flops (which are now all in FCRs) and the cells

[4]We insert input forcing circuits to 35 inputs, substitute ZPG D flip-flops for the original D flip-flops, and add footer and header cells. The details will be discussed in Section 4.

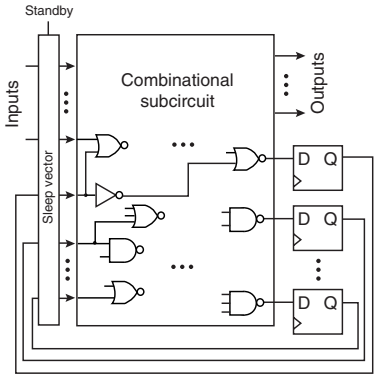

Figure 8. Sleep vector optimization.

in HCRs, which are fanins or fanouts of flip-flops, take a large proportion of the wirelength increase. Since the type of circuit rows (HCR vs. FCR) where cells are placed is determined by a sleep vector, a careful selection of sleep vector can give us a chance to reduce those wires.

As shown in Figure 8, the cells which are fanins or fanouts of flip-flops are those which we want to have in FCRs. This implies that we want to find a sleep vector that can make the outputs of all theses gates logic high, which is, in general, not possible due to conflicts (see, for example, the inverter and NOR gate). Instead, we take a heuristic approach. We apply a series of randomly generated sleep vectors, count the number of fanin and fanout gates (of flip-flops) having logic high, and then we select the best one.

For the same example circuit, we select the sleep vector out of 1000 randomly generated ones. The number of fanin and fanout cells placed in FCRs is increased from 187 (when we pick any random sleep vector) to 262. Figure 7 shows that the wirelength overhead can be reduced noticeably (from 20% to 11%).

4. Experimental Results

4.1. Design Flow

The design flow for ZPG circuits is as follows. The register transfer level (RTL) design goes through a traditional logic synthesis to create the gate-level netlist. From the netlist, we first determine the sleep vector following the method in the previous section. The sleep vector then determines the type of input forcing circuit to be inserted at each primary input. It also indicates the type of ZPG flip-flop (refer to Figure 4) to be substituted for each flip-flop in the original netlist.

Using the modified netlist, we try to determine the size (W) of a footer and a header, which affects the active-mode circuit delay. We apply random logic patterns to the inputs of the netlist and simulate it with a circuit simulator, which gives us the average current. Static timing analyzer is used while we change V_{dd} to see how much voltage drop can be tolerated to satisfy timing constraints. Then, we use the average current and voltage drop, together with turn-on resistance of a minimum-size NMOS and PMOS transistors, to obtain the size of a footer and a header [8].

In the physical design stage, we first determine the number of FCRs and HCRs from the area of cells to be placed in each type of circuit row. The footer cells and header cells are placed in a regular fashion and then fixed in their locations, followed by automatic placement and routing.

4.2. Result

We performed experiments on a set of circuits taken from the ISCAS'89 benchmarks. In Table 1, the second and three subsequent columns show the characteristics of the original circuits, which are not power-gated. The remaining columns show the area and total wirelength (normalized by those of the original circuits, respectively) of ZPG circuits. All examples are mapped on to a commercial 180nm gate library.

The sixth and seventh columns correspond to ZPG circuits, where we picked any random sleep vector and assumed that flip-flops would be placed anywhere in the placement region. The area increases by 29% on the average and the total wirelength by 28%.

When we assumed that flip-flops would be placed only in FCRs, modulated the proportion of FCRs to HCRs accordingly, and placed and routed the design again, the area overhead goes down to 9% on the average. The example s13207 benefits the most, due to its relatively large proportion of flip-flops. The wirelength remains almost the same.

When we optimized the sleep vector of each design, the wirelength overhead goes down as well (from 24% to 18% on the average). The example s13207 is an exception. Due to inherent conflict in the combinational sub-circuit (refer to Figure 8), when we tried 1000 randomly generated sleep vectors, the minimum number of fanin and fanout gates of flip-flops having logic high (which thus would be placed in FCRs) was 703 out of 1445 gates, while the maximum was 832.

5. Conclusion

Although zigzag power gating has been proposed to reduce the wakeup delay of power gating, its use of power rails in zigzag fashion has limited its use only to custom circuit design. We have proposed a power network architecture for ZPG circuits, which allows the conventional standard cells to be used without any modification. The flip-flops, input forcing circuits, and current switches have been

Table 1. Experimental result on ISCAS benchmark circuits (area and wirelength are normalized by those of original circuits)

Circuits	Original circuits				Initial P&R		FFs only in FCRs		Sleep vector opt.	
	Gates	FFs	Area (μm^2)	Wirelength (μm)	Area	Wirelength	Area	Wirelength	Area	Wirelength
s1423	925	75	8392	13174	1.27	1.26	1.09	1.27	1.09	1.20
s5378	2128	176	19305	44908	1.28	1.21	1.10	1.20	1.10	1.11
s9234	1705	145	15468	32168	1.29	1.21	1.10	1.23	1.10	1.13
s13207	5866	625	53216	124628	1.34	1.44	1.10	1.17	1.10	1.17
s35932	18603	1728	168766	436174	1.29	1.35	1.08	1.34	1.08	1.27
s38584	16031	1275	145433	405110	1.25	1.21	1.07	1.20	1.07	1.18
Average					1.29	1.28	1.09	1.24	1.09	1.18

designed to supplement the cell-based ZPG design. In order to optimize the physical design, we have proposed two methods: one to reduce the area through modulating the number of FCRs and HCRs followed by placing flip-flops in FCRs; another to reduce the wirelength via optimizing sleep vector. The proposed cell-based ZPG design with physical design optimization have been tested on several benchmark circuits.

Acknowledgment

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