Pulsed-Latch ASIC Synthesis in Industrial Design Flow

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***Abstract*— Flip-flop has long been used as a sequencing element of choice in ASIC design; commercial synthesis tools have also been developed in this context. This work has been motivated by a question of whether existing CAD tools can be employed from RTL to layout while pulsed latch replaces flip-flop as a sequencing element. Two important problems have been identified and their solutions are proposed: placement of pulse generators and latches for integrity of pulse shape, and design of special scan latches and their selective use to reduce hold violations. A reference design flow has also been set up using published documents, in order to assess the proposed one. In 40-nm technology, the proposed flow achieves 20% reduction in circuit area and 30% reduction in power consumption, on average of 12 test circuits.**

I. Introduction

A pulsed latch is a latch driven by a short pulse, rather than by a normal clock. Since the time it can capture input data is very brief, it can be approximated as a faster flip-flop. A pulse can be generated either internally or externally. In the latter approach, a single pulse generator is shared by more than one latch; it thus has advantage of area and power consumption than the former approach, and is the focus of discussion in this paper.

A pulsed latch has often been used in high performance processor designs [1]–[3], but its adoption in ASIC designs is not yet popular. Several documents have been published regarding design methodology [4] and CAD optimization [5]–[8], but the study of integrated design flow from logic synthesis to layout generation is still missing.

This paper is motivated by a question of whether commercial CAD tools, which mostly assume flip-flops as sequencing elements, can be used to design pulsed latch ASIC; some script programming may be needed where customization is necessary. The key problems have been identified during the study and solutions are provided; these include placement of pulse generators and latches for integrity of pulse shape, and design of special scan latches and their use to reduce hold violations. The proposed design flow has been compared to a reference flow. The result in 40-nm commercial technology is very positive, even though reference flow may be a little arbitrary since it itself has never been documented before in complete form: circuit area is reduced by 20% and power is consumed 30% less, on average of 12 test circuits.

A. Contributions

Our main contributions can be summarized as follows:

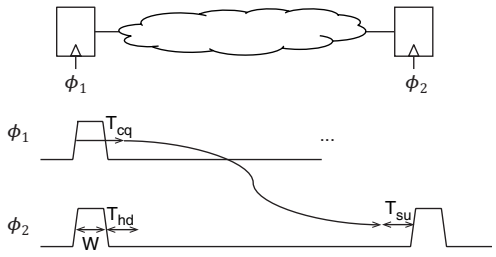

Fig. 1. Timing model of a pulsed latch circuit.

- Use of commercial CAD tools (with support of some script for customization) from RTL to layout for pulsed-latch ASIC design.
- An algorithm to insert pulse generators, and using properly sized bounding boxes for placement of pulse generators and latches.
- Design of special scan latches and an algorithm for their selective use to reduce hold violations.

The remainder of this paper is organized as follows. In Section II, we discuss how the timing model of standard latch is altered so that pulsed latch can be used right from the logic synthesis stage. A new pulse generator is proposed, in which output pulse is not distorted even when input clock transitions slowly; it is further modified to have pulse enable input, so that it is used during clock gating synthesis. The problems of pulse generators insertion and automatic placement are addressed in Section III. Special scan latches are proposed in Section IV; how they are used together with standard scan latches are presented with the objective of minimizing hold violations. Experimental results are presented in Section V and we draw conclusions in Section VI.

II. Preliminaries

We assume a standard ASIC design process as a base of proposed flow; it consists of a sequence of logic synthesis (which also performs clock gating synthesis), test synthesis, placement, clock tree synthesis, and routing.

A. Timing Model

The foundation of using a pulsed latch in ASIC design is to treat it as a faster flip-flop. This is made possible by forcing that data arrives before the rising edge of pulse, which implies that setup margin (T_{su}) and clock-to-Q delay (T_{cq}) are

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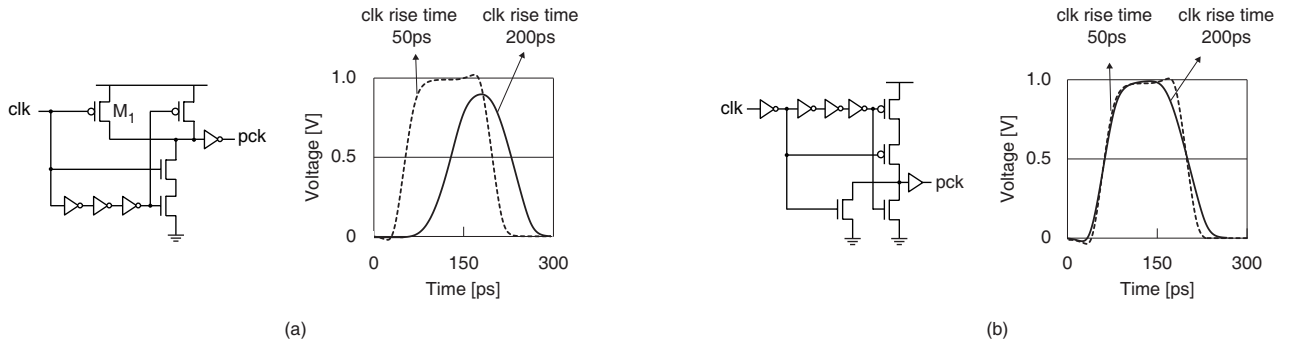

Fig. 2. (a) A pulse generator [1] and (b) its modified form. The pck waveforms are shown for two different clk rise times.

characterized at the rising edge as shown in Fig. 1, and data-to-Q delay of standard latch is not used. Time borrowing is inhibited as a result; the amount of time allocated to each latch to latch path is fixed to a clock period as in flip-flop circuits. Logic synthesis can be performed while latches are treated as flip-flops, and we take advantage of smaller sequencing overhead.

While the second latch is transparent ($\phi_2 = 1$ in Fig. 1), its input, which is on the path from the first latch, has to stay stable. The hold margin (T_{hd}) is thus characterized at the falling edge of pulse, and minimum delay between latch pairs d_{12} has to satisfy

$$T_{cq} + d_{12} \geq W + T_{hd}, \tag{1}$$

where W is pulse width. Due to the presence of W, (1) implies a risk of more hold violations than in a flip-flop circuit and thus more extra delay buffers, which requires a special attention, a topic discussed in more details in Section IV.

B. Pulse Generator

A pulse generator is a key circuit component. One of its implementations [1], which we base on, is shown in Fig. 2(a). A drawback of this pulse generator is distortion of pulse pck as input clock clk transitions slowly, as indicated by SPICE waveforms; this is because slow transitions directly drive pMOS transistor M_1.

The pulse generator was modified by inserting an inverter at clk input, so that clock signal can be regenerated, and by adopting an NOR structure accordingly, as illustrated in Fig. 2(b). The SPICE waveforms confirm that pck is not distorted now even when rise time of clk is 200 ps; this however comes at the cost of 4.8% increase of cell area and 29.7% increase in power consumption.

1) Pulse Generator with Pulse Enable: The basic pulse generator can be extended to a generator with pulse enable, as illustrated in Fig. 3(a). The new generator can be used instead of a clock gating cell (CGC) as shown in Fig. 3(b); this allows us to set the new generator as a CGC and perform a standard clock gating synthesis. Notice that the latch within CGC is not necessary any more. This is because glitches at en arising when clk is 1 are unlikely to affect pck (see the waveforms of Fig. 3(a)), because a pulse is very short and minimum delay of en is usually larger than pulse width, or we force minimum delay to be larger than pulse width.

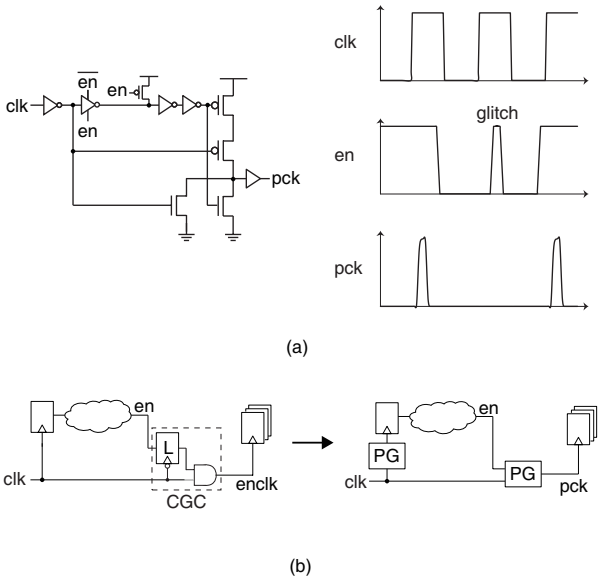

Fig. 3. (a) Pulse generator with pulse enable and (b) its use in clock gating in place of a clock gating cell.

III. Pulse Generators Insertion and Placement

It is important to assure that pulse is delivered from each pulse generator to connected latches without distortion. This is accomplished by characterizing maximum load capacitance that a generator can support, called load limit, and make it sure that actual load does not exceed this limit.

The load of pulse generator is determined by the number of attached latches and the wiring for connection. Thus, pulse generators insertion and placement are two steps to be addressed in this context.

A. Design Flow

The overall flow of the steps is illustrated in Fig. 4. As explained in the previous section, clock gating synthesis is performed while pulse generator with pulse enable is used instead of CGC. Thus, the latches in which clock gating is performed, called gated latches, are already attached to generators, while ungated latches are not. A bounding box is assigned to each group of gated latches and their generator, so that they remain inside the box during automatic placement, while load limit of pulse generator is honored.

Pulse generators are inserted to ungated latches using a simple greedy algorithm. Let each latch belong to its own

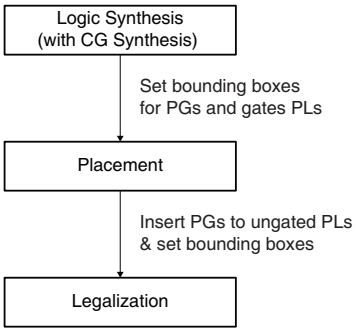

Fig. 4. Pulse generators insertion and placement flow.

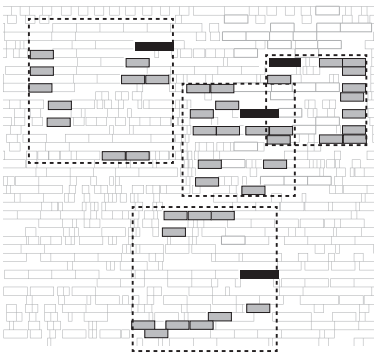

Fig. 5. Example layout of a test circuit wb_dma after placement with bounding boxes.

group. We determine two groups i and j with minimum wiring cost and merge the two into a single group; the wiring cost is the length of Steiner tree that spans all the latches of i and j subtracted by Steiner tree length of i and that of j. The process iterates until no two groups can be merged; a pulse generator is then assigned to each group and connections are made to member latches.

We limit the number of latches that can be grouped to 11. This is determined in empirical fashion: too small number yields large number of pulse generators; too large number causes bad placement since a pulse generator and member latches are clumped together due to less budget on wirelength. A bounding box is assigned to each group of ungated latches and pulse generator, and legalization is performed so that group members are moved to inside the box boundary. Fig. 5 is an example layout after placement.

B. Sizing Bounding Boxes

The size of each bounding box should be properly set in a way that the load of pulse generator does not exceed its load limit, irrespective of location of generator and latches inside the box.

The pulse generator is loaded by latch and wire capacitance. As it drives more latches, there is less budget for wire capacitance, which implies a shorter distance being allowed between pulse generator and latches. This is experimentally demonstrated in Fig. 6. The y-axis corresponds to maximum distance between pulse generator and latches when their connections are made using Steiner tree (see thick line between generator and latch in Fig. 6). Note that this value varies

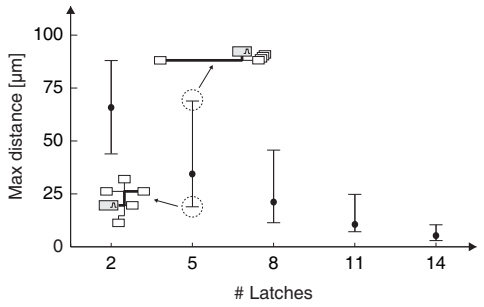

Fig. 6. Maximum distance between pulse generator and latches under 15 fF of load limit. Maximum, minimum, and mean values are shown for some number of latches.

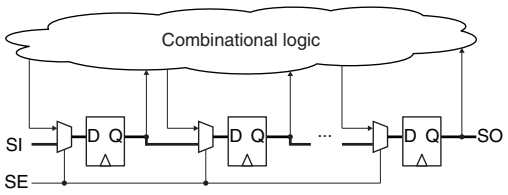

Fig. 7. A scan chain. Thick line corresponds to a scan signal path. SI, SO, and SE are scan input, scan output, and scan enable, respectively.

for a given number of latches depending on how latches are distributed in a plane and how much wires are shared in Steiner tree.

A square bounding box is assumed, whose length of diagonal line is empirically set to twice the mean value of Fig. 6. After placement, the load of each generator is examined; if it exceeds the load limit, a square is reduced by setting the length of diagonal to twice the minimum value of Fig. 6, which is then followed by legalization.

IV. Scan Design

Pulsed-latch circuit is susceptible to hold violations as dictated by (1). Scan signal path, which is illustrated by a thick line in Fig. 7, is particularly very susceptible since the path contains few logic gates. The extra buffers inserted to fix hold violations may mask out the benefit of using pulsed latches.

We have designed two special scan latches, so that they, together with standard scan latch, can selectively be used in a design in a way that hold violations are minimized.

A. Scan Latch Design

Fig. 8(a) is a standard scan latch; Q corresponds to data output in normal operation (SE = 0) and scan output during scan operation (SE = 1) in the setting of Fig. 7. In Fig. 8(b), Q is now dedicated to data output while scan output is available at additional pin $\overline{\text{SQ}}$; the polarity of scan output is now opposite, which can be taken care of while test patterns are prepared. Notice that $\overline{\text{SQ}}$ is asserted after the falling edge of pulse as shown in SPICE waveforms, which increases minimum delay along the scan path thereby reducing the risk of hold violations. This however comes at the cost of 8% increase of cell area. Fig. 8(c) is similar to Fig. 8(a), and Q' is used both for data and scan output; the difference is that Q'

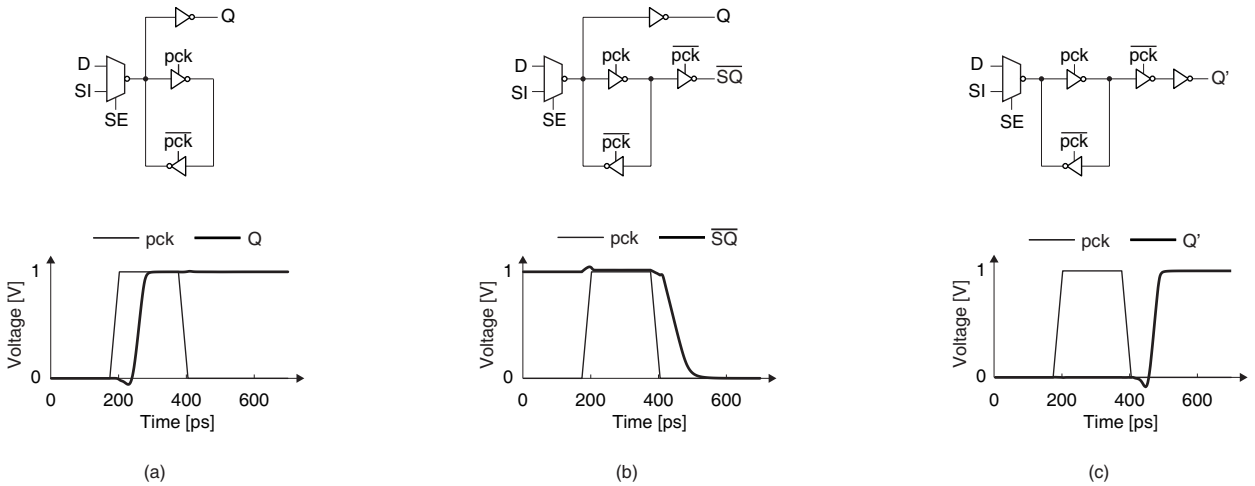

Fig. 8. (a) A standard latch, (b) a latch with delayed scan output, and (c) a latch with delayed data output.

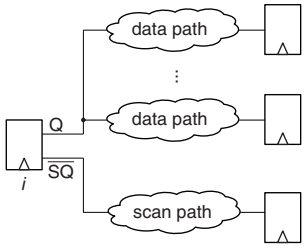

Fig. 9. Data paths and a scan path launched from a latch i.

is delayed and available after the falling edge of pulse, which is conceptually similar to Fig. 8(b). The area of this latch is also 8% larger than that of standard latch.

B. Scan Latch Selection

In the proposed design flow, logic synthesis, placement, and clock tree synthesis are all performed using latches with delayed scan output (Fig. 8(b)). For each latch i, we now determine whether it benefits if i is replaced by other latch types (a standard latch or a latch with delayed data output). The objective is to minimize the area sum of i and extra buffers that must be inserted to fix hold violations in the path launched from i.

Consider Fig. 9; a latch i usually launches more than one data path but only one scan path. If there are no hold violations on data paths, we check scan path. If hold slack on the scan path is positive enough such that even a standard latch does not cause hold violation, i is replaced by a standard latch for benefit of smaller latch area; otherwise no action is taken. If data paths involve hold violations and setup slack is positive enough such that a latch with delayed data output can be deployed without causing setup violation, i is replaced to that latch type; otherwise a standard latch and a latch with delay scan output are compared in terms of latch area and resulting buffers area, and the one that results in smaller area is taken.

V. Experimental Results

A set of test circuits was prepared using ITC benchmarks and open cores [9]. They are listed in Table I. All experiments were performed using 40-nm industrial library. The proposed design flow was implemented using Tcl script, which is executed on commercial CAD tools; specifically, pulse generators insertion, bounding box assignment, and scan latch selection were implemented. A pulse generator was designed for pulse width of 210 ps in worst process corner (110 ps in best corner). Its load limit is 15 fF; maximum fanout is set to 11 latches, which correspond to about 10 fF.

TABLE I
Test circuits

Name	# Gates	# SEs	Clock period (ns)
b12	1000	121	1.5
b14	3461	247	4.2
b17	21191	1415	2.9
ac97ctrl	8020	2199	2.2
aes_core	14402	530	2.8
des	2164	190	2.3
memctrl	8674	970	2.6
or1200	10812	788	6.3
spi	2487	229	2.4
tv80	5604	359	2.3
usb	9164	1746	3.3
wb_dma	2272	563	2.0

A. Reference Design Flow

To assess the proposed design flow, a reference design flow was set up [4], [10]. An initial netlist is generated using flip-flops; it is then submitted to automatic placement. The critical path delay is measured and is assumed to be a clock period, which is reported in the last column of Table I. The load limit of clock gating cell (CGC) is deliberately set to 15 fF, which is the same as the load limit of pulse generator, during clock gating.

After placement, all flip-flops are replaced by latches, and each CGC is replaced by a pulse generator with pulse enable (Fig. 3(a)). To insert pulse generators for ungated latches, clock tree synthesis is performed while the load limit of leaf-stage clock buffer is set to that of pulse generator; each buffer is then replaced by a pulse generator and the clock

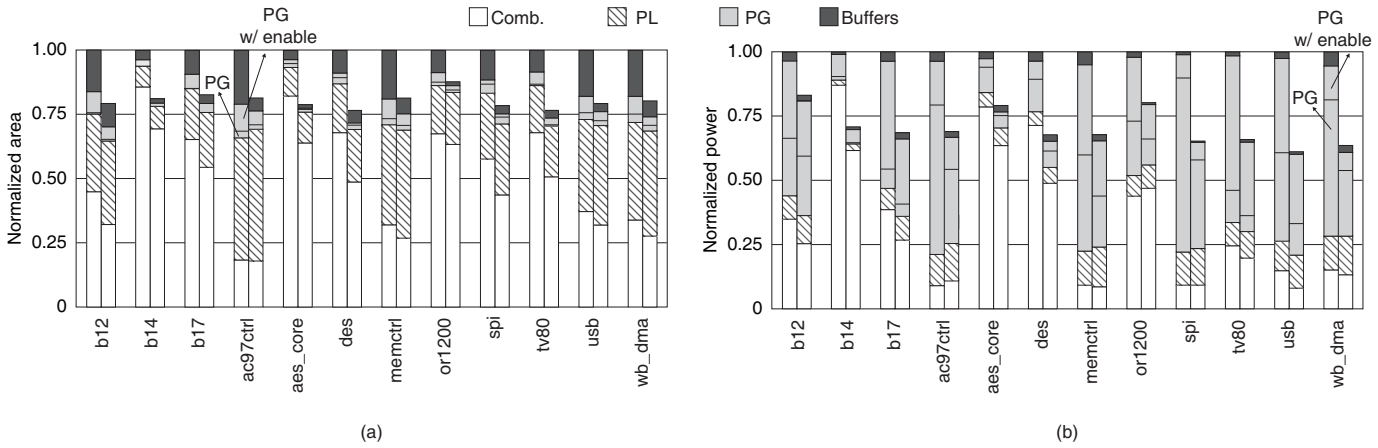

Fig. 10. Comparison of reference flow (left bars) and proposed flow (right bars): (a) circuit area and (b) power consumption.

tree beyond pulse generators are removed. A clock tree is synthesized once again with pulse generators as sinks; hold violations are checked and delay buffers are inserted where they are necessary; and routing is performed to finalize layout. Only standard latches (see Fig. 8(a)) are assumed during test synthesis.

B. Comparison of Reference and Proposed Design Flow

1) Circuit Area: Sum of standard cell areas is compared between the reference and proposed design flow in Fig. 10(a). The proposed flow achieves 19.8% reduction on average. This is due to three factors:

- Logic synthesis is performed using flip-flops in the reference flow, but using latches in the proposed flow. Since sequencing overhead of latch (57 ps) is much smaller than that of flip-flop (159 ps), synthesis yields less combinational logic in the proposed flow for the same clock period.
- Less number of pulse generators are used due to more efficient pulse generators insertion procedure (see Section III-A and Section V-A).
- Selective use of three scan latches yields substantially less number of hold violations and smaller number of extra buffers.

2) Power Consumption: Power consumption (including both switching and leakage) was measured using fast transistor-level simulator, while 100 randomly generated patterns are provided at inputs; thus power consumption we report corresponds to that while circuit is actively switching. The result is shown in Fig. 10(b), which indicates 29.8% reduction in the proposed flow. Main saving comes from pulse generators as well as from combinational logic. Comparing the portion of generators in Fig. 10(a) and (b) reveals their importance in power consumption. A generator consumes about 10 μW; this is 58 and 12 times of power consumption of 2-input NAND gate and a latch, respectively.

A portion of pulse generator in Fig. 10 is divided into a basic pulse generator (PG) and a generator with pulse enable (PG with enable). Since PG is never gated, it represents a source of large power even though it occupies a small area.

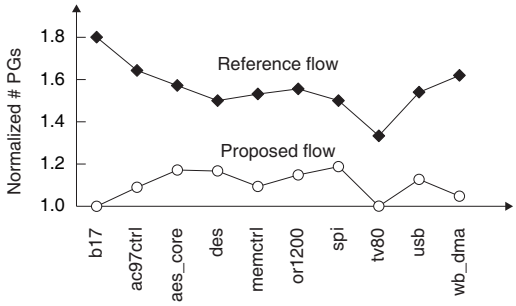

Fig. 11. The number of pulse generators (normalized) inserted for ungated latches.

C. Analysis of Pulse Generators Insertion and Placement

The numbers of pulse generators from reference and proposed flow are compared in Fig. 11; the pulse generators for gated latches are same in both flows and are dropped; b12 and b14 use only one or two generators, and are not included in the comparison. We also obtain the number of pulse generators with zero wire capacitance, and regard that number as a (loose) lower bound, which is used to obtain normalized numbers of Fig. 11. The average of reference flow is 1.55 while that of proposed flow is 1.09. Considering that the bound is lower than the actual minimum (which is unknown), the proposed heuristic is efficient even though it is a simple greedy.

We use bounding boxes during placement to force pulse generators and latches to be placed nearby. Another method to achieve this goal is to assign higher net weight in their connections, even though there is no guarantee that load limit of pulse generators is honored. Two placement methods are compared in Fig. 12, in terms of total wirelength as a way of assessing placement quality.

Another placement is created without restriction on the location of pulse generators and latches; total wirelength is measured, and is used to normalize the wirelength from the two methods. The average of net weighting is 1.09 while that of bounding box is 1.03, which shows the benefit of using bounding boxes.

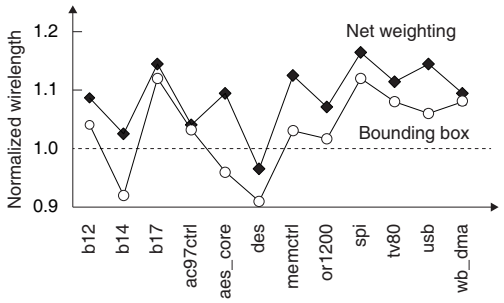

Fig. 12. Comparison of total wirelength of placement using net weighting and bounding boxes.

TABLE II

THE NUMBERS OF HOLD VIOLATIONS IN REFERENCE AND PROPOSED FLOW; PERCENTAGE USE OF SCAN LATCH TYPES IN PROPOSED FLOW

Name	# Hold violations		Percentage of latch types		
	Reference	Proposed	Standard	Delayed $\overline{SQ}$	Delayed Q
b12	235	162	1.7	20.7	77.7
b14	266	93	0.9	83.5	15.8
b17	1899	784	1.7	57.5	40.8
ac97ctrl	3075	1684	1.8	26.9	71.3
aes_core	489	166	1.1	74.5	24.3
des	316	147	6.3	66.8	26.8
memctrl	1755	634	1.1	41.5	57.4
or1200	1277	623	2.1	27.8	70.2
spi	403	122	1.7	25.8	72.5
tv80	576	212	3.3	35.9	60.7
usb	2795	1084	1.0	28.6	70.4
wb_dma	896	373	1.7	35.8	62.5
Avg	1.0	0.43	2.0	43.8	54.2

D. Analysis of Scan Design

The number of hold violations before delay buffers are inserted is compared in columns 2-3 of Table II; it is apparent that hold violations are substantially reduced by employing newly designed scan latches. The extent of hold slack being negative, not simply the number of hold violations, is important. Fig. 13 reports two hold slack histograms of b14, one at data outputs and the other at scan outputs; the benefit of new scan latches is also clear in this context.

The last three columns of Table II show the percentage of scan latches that are used in the proposed flow. As expected, standard latches are rarely used since employing them causes large amount of negative hold slacks in most scan paths. As we have described in Section IV-B, an initial netlist is made using only the latches with delayed $\overline{SQ}$, i.e. data output is available at Q and scan output is available at $\overline{SQ}$. While we determine scan latch type for each latch, if hold slack at Q is negative, there is high chance that that latch is replaced by a latch with delayed Q. This conjecture is well confirmed in Fig. 14.

VI. CONCLUSION

We have presented an integrated design flow based on commercial CAD tools, with support of some script to customize pulse generators insertion, placement of pulse generators and latches, and optimizing scan chain to reduce hold violations.

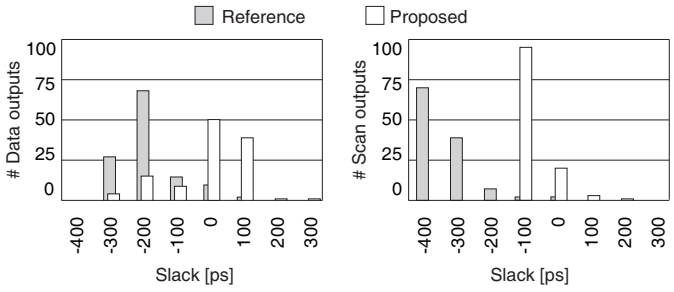

Fig. 13. Hold slack histograms of a test circuit b14.

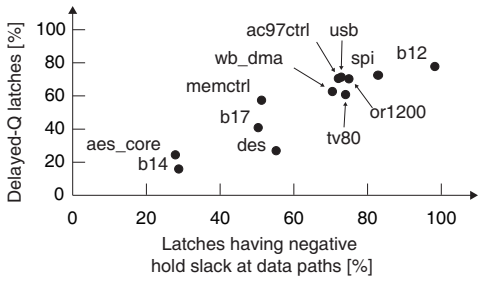

Fig. 14. Latches having negative hold slack at data paths (before scan latch selection) versus percentage use of latches with delayed-Q after scan latch selection.

The benefit of proposed design flow in circuit area and power consumption has been demonstrated using 40-nm commercial library. A future plan includes a validation of proposed flow through test chip.

ACKNOWLEDGMENT

This work was supported in part by the Mid-Career Researcher Program through NRF Grant funded by the MEST (2011-0029087), and by LG Electronics.

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