Analysis and Minimization of Short-Circuit Current in Mesh Clock Network

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***Abstract*— Mesh clock network is very effective at reducing clock skew. But mesh causes a large increase of power consumption, in particular due to shorted buffers. We first analyze the short-circuit power consumption of the mesh clock network. It is observed that skew distribution of premesh tree is important in determining the amount of short-circuit power. We then propose a new clock buffer, which practically eliminates short-circuit current in a mesh network. Experiments on a few test circuits using 40-nm technology indicate that clock power consumption is reduced by 13.0% on average with 4.8% of area increase; this can be compared to buffer sizing, which only achieves 5.6% saving of power.**

I. Introduction

Tree and mesh are two popular structures of clock distribution network. Tree is more commonly used in ASIC design. It is however very susceptible to on-chip process variations [1], which leads to large amount of clock skew. Mesh has been widely used in high performance processor designs [2] for smaller skew. Its structure is illustrated in Fig. 1. Clock sinks, such as flip-flops, are driven by postmesh buffers to ensure proper amount of clock transition time; postmesh buffers are then connected to mesh through stubs; a premesh tree then connects a clock source to mesh. A spine structure may be used instead of mesh [3]. A tree may be modified to reduce skew by shorting some buffers [4], which shares the same motivation of mesh.

Clock distribution network consumes large amount of power, e.g. 40% of total power in microprocessors [5]. Power consumption is even more important in mesh due to substantial use of wires. A component of power that draws a particular attention is short-circuit current. This can easily be understood by referring to Fig. 2, which shows two leaf-stage clock buffers (LCBs) of premesh tree connected to mesh. If clock falls earlier in one LCB, a path of short-circuit current establishes as indicated in Fig. 2. The period of time the two LCBs are shorted is determined by skew of premesh tree.

One method to reduce short-circuit current is buffer sizing [6]. In Fig. 3(a), if clock arrives later at the first LCB (than at the second) and earlier at the third, buffer sizing is performed at the two LCBs so that short-circuit current is reduced. The extent of sizing is determined by how much clock arrives later or earlier. The extra capacitor may be added to compensate for the decreased buffer capacitance, so that the load of buffers driving LCBs remains unchanged.

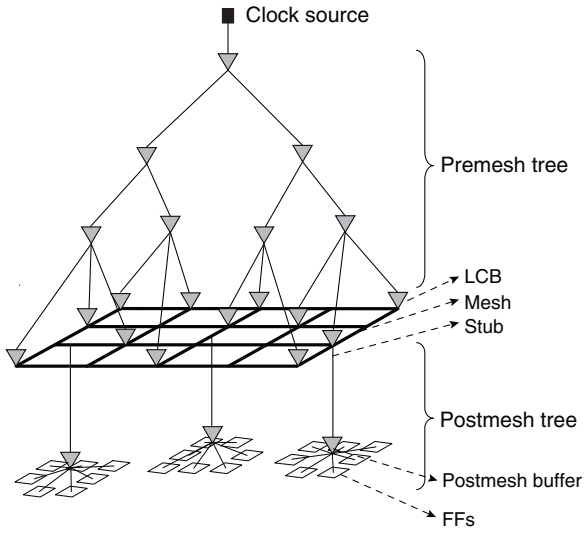

Fig. 1. Structure of mesh clock network.

Another method, named high impedance buffer (Hi-Z buffer) [7], is illustrated in Fig. 3 (b). Two extra buffers are inserted before pMOS and nMOS transistors; the buffer in front of pMOS is fast when 1 is propagated but slow for propagating 0; the opposite is true in the buffer in front of nMOS. It is easy to see that the period when both pMOS and nMOS are turned off is extended both for rising and falling input, which helps reduce short-circuit current.

Our main contributions in this paper are as follows.

- Analysis of short-circuit current of mesh clock network (Section II.A and II.B), which indicates that short-circuit current increases as the standard deviation of premesh skew increases.
- A new clock buffer, which practically eliminates short-circuit current, and its assessment (Section III); clock power consumption decreases by 13.0% on average of 10 test circuits with 4.8% of area overhead.

II. Analysis of Short-Circuit Current

Two test circuits from open cores [8], ac97_ctrl and usb_funct, were taken for the experiment. Each circuit was synthesized and placed using 40-nm industrial library. Postmesh

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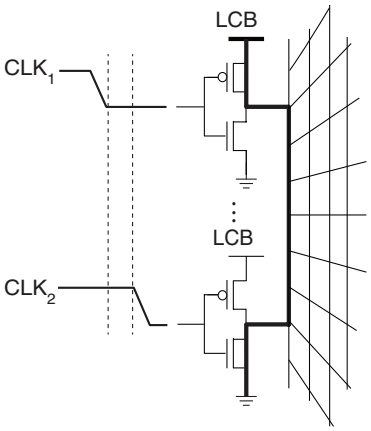

Fig. 2. Short-circuit current in mesh clock network.

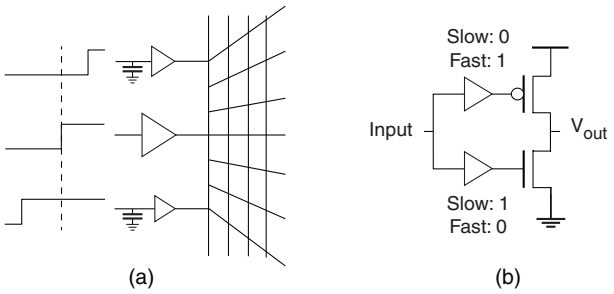

Fig. 3. Prior methods to reduce short-circuit current of mesh clock network: (a) buffer sizing and (b) Hi-Z buffer.

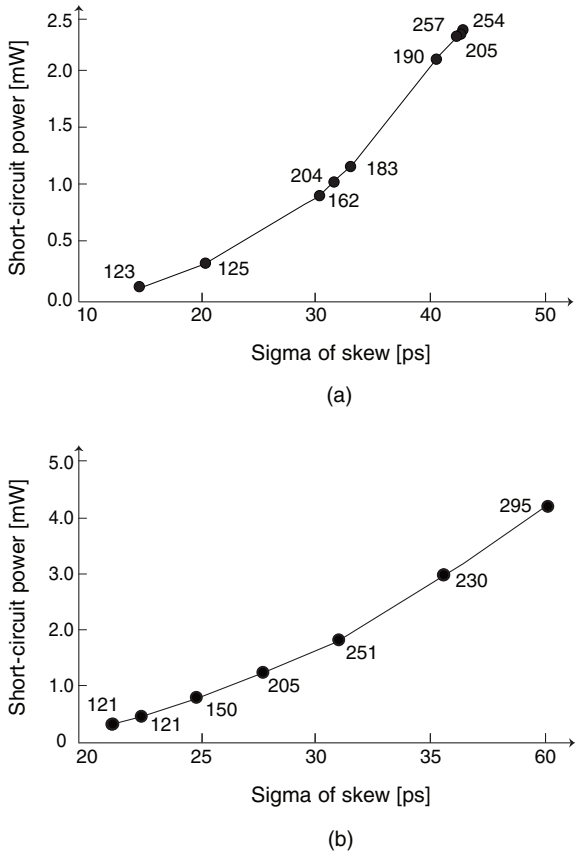

Fig. 4. Short-circuit power consumption of LCBs vs the standard deviation (sigma) of premesh skew: (a) ac97_ctrl and (b) usb_funct.

buffers (see Fig. 1) are inserted and connected to local flip-flops in a way that the clock transition time of all flip-flops remains below 150 ps. A placement area dictates the mesh size. The numbers of columns and rows are determined in such a way that total wirelength including mesh and stub is minimized. The total capacitance of resulting mesh, stubs, and postmesh buffers yields the number of LCBs that are placed. Premesh tree synthesis is then performed to finalize the clock network; maximum skew is a parameter that we adjust for this process.

A. Short-Circuit Current vs Premesh Skew

Fig. 2 implies that premesh skew is important in determining the amount of short-circuit current through LCBs. Specifically, it has been experimentally shown [7] that the short-circuit current increases as premesh skew increases.

This, however, is not exactly the case as our experiment demonstrates in Fig. 4. The x-axis is the standard deviation of premesh skew; the maximum skew value is also denoted along the graph. Note that there exists a great difference of short-circuit power for some maximum skew values that are close, e.g. 204 vs 205 in Fig. 4(a). Instead, short-circuit power increases as the standard deviation of premesh skew increases, which is also confirmed in Fig. 4(b). This is an understandable consequence since more LCBs will incur short-circuit current in longer period of time if skews are more widely distributed.

B. Short-Circuit Current vs Placement Area

Utilization is an important parameter in automatic placement. A low utilization allows easier routing and low congestion but at the cost of larger placement area; it may cause more clock power consumption due to larger mesh and more number of buffers. We took usb_funct, performed placement with two different utilizations (50% and 70%), constructed mesh clock network while we adjust the target maximum skew of premesh tree as in Section II.B, and measured clock power consumption (both total and short-circuit).

The results are shown in Fig. 5. The placement with 50% utilization consumes about 20% more total clock power than the one with 70% utilization; it is associated with wider distribution of power (over sigma of premesh skew) due to enlarged placement area.

Short-circuit power is insignificant portion of total power when skew sigma is small, e.g. 4% for skew sigma of 21 ps when placement utilization is 50%; it however becomes substantial as skew sigma increases, e.g. 34% for skew sigma of 58 ps. It is also noted that short-circuit power increases more rapidly in 50% placement utilization, since more LCBs are involved in short-circuit current.

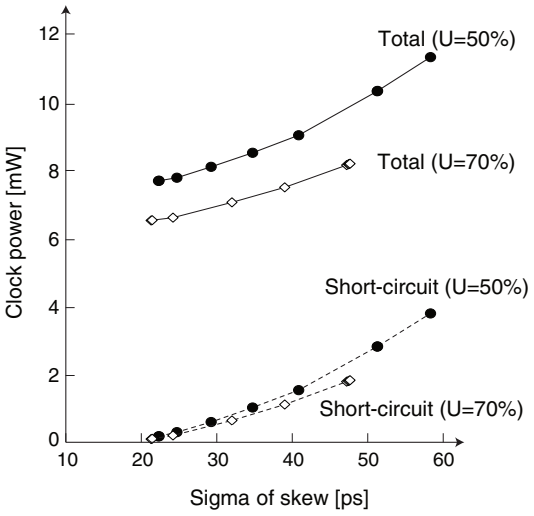

Fig. 5. Total and short-circuit clock power as sigma of premesh skew varies.

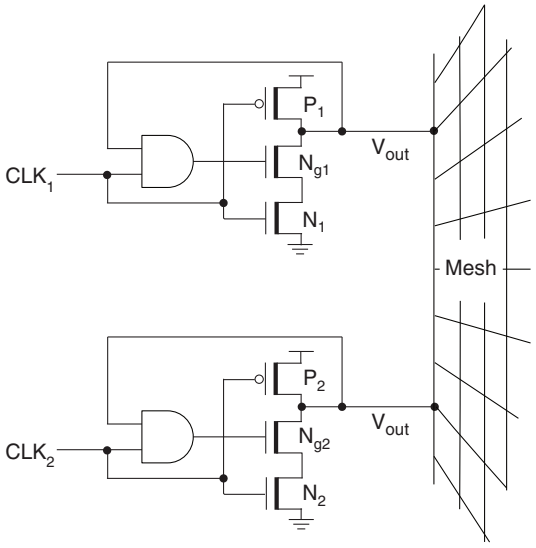

Fig. 6. Short-circuit blocking buffers.

III. New LCB for Smaller Short-Circuit Current

A. LCB Design

A new LCB, which we name as short-circuit blocking buffer (SBB), is shown in Fig. 6 (two SBBs are shown for illustrative purpose); it consists of extra nMOS transistor N_g and AND gate in addition to inverting buffer made of P and N. Consider a single SBB first. If input clock is 0, N_g and N are turned off while P is turned on and charges V_{out} to V_{dd}. If clock rises, P is turned off and N is turned on; since both V_{out} and clock are 1, N_g is temporarily turned on and starts discharging V_{out}; the delay from V_{out} to AND gate output is intentionally made larger so that N_g stays turned on as long as possible during discharge process. Fig. 7 shows the waveforms of clock, the output of AND gate, and V_{out} after SPICE simulation. SBB was designed in 40-nm technology and compared to a standard inverting buffer with equal driving strength. It occupies 2.8 times of standard buffer area and consumes about 10% more power. The advantage, however, is almost zero short-circuit current when SBBs are used as LCBs.

Consider now two SBBs as illustrated in Fig. 6. Assume that CLK_1 falls earlier than CLK_2 does. While CLK_1 is 0 and CLK_2 is still 1, both P_1 and N_2 are turned on but N_{g2} is turned off blocking short-circuit current path. If CLK_1 rises earlier than CLK_2 does, N_{g1} blocks short-circuit current path this time from P_2 through N_1.

B. Design of Mesh Clock Network Using SBBs: Assessment

Mesh clock network was designed using SBBs for a few test circuits listed in Table I, and was compared to the network using Hi-Z buffers and relying on buffer sizing (see Section I). Initial network, which serves as a reference of comparison, was constructed by using standard inverting buffers as LCBs and following the procedure in Section II; each LCB was then replaced by SBB (or replaced by Hi-Z buffer or downsized).

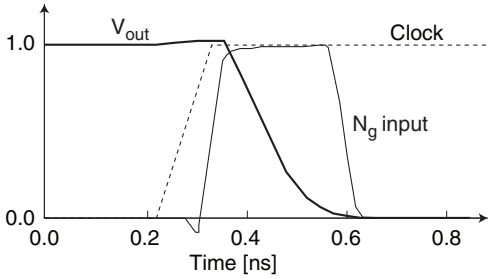

Fig. 7. SPICE simulation of SBB.

1) Clock Power Reduction: The percentage reduction of total clock power consumption of three methods is reported in columns 2–4 of Table II. SBB reduces clock power on average of 13%, which can be compared to 2.6% from Hi-Z buffers and 5.6% from buffer sizing. Specifically, short-circuit current is almost removed in SBB, but buffer sizing can only reduce it by 27.6% on average.

In tv80, power consumption increases rather than decreases (both in SBB and Hi-Z buffer). This is because short-circuit current is not large enough, so the increased power of buffers (20.7% in Hi-Z buffer and 10.0% in SBB) outweighs the saving in short-circuit power. This can also be understood from relatively smaller premesh skew of tv80 shown in the last column of Table I, which will lead to smaller short-circuit current as we discussed in Section II.

2) Area Overhead: SBB occupies 2.8 times of standard buffer area; Hi-Z buffer occupies 4.2 times. We want to understand how much chip area increases if these two buffers are employed as LCBs. Columns 5–6 of Table II indicate that SBB causes 4.8% increase of area (as measured by total cell areas) on average; Hi-Z buffers causes 8.9% increase.

TABLE II

COMPARISON OF SBB, HI-Z BUFFER, AND BUFFER SIZING TO REDUCE SHORT-CIRCUIT CURRENT

Circuit	Clock power reduction (%)			Area overhead (%)		Stability (%)	
	SBB	Hi-Z buffer	Buffer sizing	SBB	Hi-Z buffer	SBB	Buffer sizing
tv80	-5.8	-20.7	1.0	5.2	9.6	1.7	9.0
systemcaes	14.4	2.1	2.2	4.3	8.0	2.4	4.7
mem_ctrl	12.6	-0.2	8.8	6.2	11.5	3.0	4.8
ac97_ctrl	17.4	7.3	9.3	5.9	10.9	2.5	5.2
usb_funct	23.0	14.1	9.5	5.7	10.6	1.6	4.5
s38417	2.1	-6.4	3.0	5.8	10.7	1.9	7.1
wb_conmax	21.0	9.6	6.8	2.7	5.0	1.8	5.4
aes_core	17.5	7.6	4.3	4.0	7.4	1.8	4.8
pci_bridge32	5.6	-0.9	4.1	5.3	9.8	1.8	4.7
b17	21.9	13.2	7.1	3.2	5.9	1.9	4.5
Average	13.0	2.6	5.6	4.8	8.9	2.0	5.5

TABLE I

TEST CIRCUITS

Circuit	# Gates	# FFs	# LCBs	Premesh skew (ps)
tv80	7161	359	225	140
systemcaes	7959	670	289	216
mem_ctrl	11440	1083	400	228
ac97_ctrl	11855	2199	529	257
usb_funct	12808	1746	529	226
s38417	8278	1564	529	200
wb_conmax	29034	770	442	220
aes_core	20795	530	625	240
pci_bridge32	16816	3269	841	243
b17	21191	1407	576	204

We may take a hybrid approach in a way that some LCBs are implemented by using SBBs while the remainders are realized using standard buffers. The objective will be to minimize short-circuit current and to keep the area overhead as small as possible. The new approach is left for future investigation.

3) Stability to Process Variation: Premesh skew is altered by on-chip process variation, which in turn affects short-circuit power consumption. This can be assessed by measuring total clock power consumption with Monte Carlo simulation, which was repeated 200 times in our experiment.

The percentage increase of total clock power with corresponding numbers used in columns 2 and 4 as references is reported in the last two columns of Table II, which we denote as stability. It is clear that SBB method is more stable than buffer sizing. This is mainly because short-circuit current is practically eliminated in SBB, but large amount of it still remains in buffer sizing. Specifically, in buffer sizing, due to process variation, short-circuit power consumption increases by 22.8% on average (as high as 81.6%).

IV. CONCLUSION

We have performed analysis of short-circuit current in mesh clock network. Experiments have shown that the standard deviation of premesh skew is an indicator of short-circuit current; it has also been shown that short-circuit current (and total clock power consumption) rapidly increase as placement area increases. A new clock buffer, SBB, has been proposed to eliminate short-circuit current. Its application to practical mesh clock network has been demonstrated in 40-nm technology; its impact on clock power consumption and chip area has been assessed.

Premesh tree needs to be synthesized such that skew sigma becomes smaller, which then leads to smaller short-circuit current. Using both standard buffers and SBBs as LCBs allows minimizing both short-circuit power and chip area. Both can be pursued as future research.

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REFERENCES

[1] J. Xi and W. Dai, "Buffer insertion and sizing under process variations for low power clock distribution," in *Proc. Design Automation Conf.*, June 1995, pp. 491–496.

[2] S. Tam, S. Rusu, U. Desai, R. Kim, J. Zhang, and I. Young, "Clock generation and distribution for the first IA-64 microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 11, pp. 1545–1552, Nov. 2000.

[3] G. Gerosa and H. Samarachi, "A sub-1W to 2W low-power IA processor for mobile internet devices and ultra-mobile PCs in 45nm Hi-K metal gate CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 256–611.

[4] A. Rajaram, J. Hu, and R. Mahapatra, "Reducing clock skew variability via crosslinks," in *Proc. Design Automation Conf.*, June 2004, pp. 18–23.

[5] P. Gronowski, W. Bowhill, R. Preston, M. Gowan, and R. Allmon, "High-performance microprocessor design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 676–686, May 1998.

[6] G. Wilke and R. Reis, "A new clock mesh buffer sizing methodology for skew and power reduction," in *IEEE Computer Society Annual Symp. on VLSI*, Apr. 2008, pp. 227–232.

[7] G. Wilke, R. Fonseca, C. Mezzomo, and R. Reis, "A novel scheme to reduce short-circuit power in mesh-based clock architecture," in *Proc. Annual Symp. on Integrated Circuits and System Design*, Sept. 2008, pp. 117–122.

[8] "Opencores," http://www.opencores.org/.