

Pulsed- V_{dd} : Synchronous Circuit Design without Clock Network

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Abstract—Almost all digital circuits designed these days are synchronous ones. A clock is responsible for synchronization and is distributed via clock (distribution) network, which requires significant design time and effort and incurs extra area and wirelength. We advocate that synchronous circuit can be designed without clock network. Instead, power supply V_{dd} network is made to carry periodic negative pulses. A new sequencing element is proposed, which internally generates a positive pulse with each negative pulse on V_{dd} and then latches input data using that pulse. Since pulses are delivered over the V_{dd} network, which inherently has small RC value, skew becomes smaller, which is another advantage.

I. INTRODUCTION

Clock network is a key component in synchronous circuit, and the design of high quality network requires substantial effort. Hybrid clock mesh and tree has become popular to reduce clock skew; however, more area is occupied by network wires when compared to simple clock tree, e.g. two to three times [1]. Clock tree is very susceptible to on-chip process variations [2], which is another reason why mesh structure has become popular. It is well known that clock network is the largest source of power consumption, e.g. about 40% in typical processors [3].

Asynchronous circuit is implemented without clock network but it has its own limitations [4]: about 20% more area is needed, in general, compared to synchronous counterpart, all signals have to be free from hazards, and commercial CAD tools do not support its design.

It would be a great benefit if we are able to keep designing synchronous circuits using established design methodologies and CAD tools, but without clock network. The question is how synchronization is maintained.

II. OVERVIEW

The concept of pulsed- V_{dd} that we propose is illustrated in Fig. 1(a). There is no clock network, so sequencing elements do not have clock inputs. A power supply, denoted by PV_{dd} , carries periodic negative pulses as shown in Fig. 1(b). The details of PV_{dd} generation and its distribution will be studied in the future as we continue to develop the concept.

The key component is a pulse generator (generator for short), which generates a positive pulse (denoted by pck in Fig. 1(b)) in accordance with each PV_{dd} pulse. It then triggers a latch to capture input data; thus, the latch in this case behaves as a pulsed latch. A generator may be shared by more than

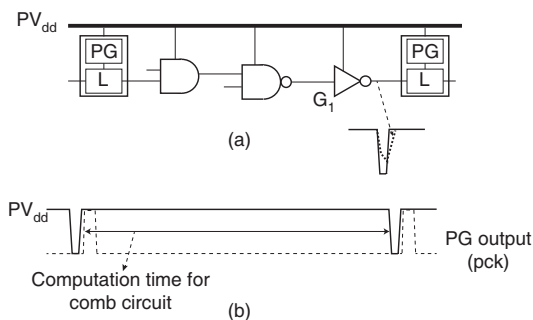


Fig. 1. (a) A concept of pulsed- V_{dd} and (b) PV_{dd} and pck waveforms.

one latch, but we assume an integrated generator and latch in this paper.

Consider a fanin gate of latch, G_1 in Fig. 1(a). If its output is 0, it is not affected by PV_{dd} pulse. The output of 1 is affected, but it is restored as the pulse rises (see Fig. 1(a)); note that the input is 0 in this case, which is unaffected. This applies to all CMOS gates, which are inverting logic (even non-inverting gate such as AND is internally inverting). If the gap between rising edge of PV_{dd} pulse and that of pck is larger than setup constraint of latch, the output of G_1 is captured at the rising edge of pck. Computation has to be completed before the next PV_{dd} pulse as shown in Fig. 1(b), so the width of PV_{dd} pulse is wasted.

III. PULSED LATCH DESIGN

A pulse generator is shown on the left of Fig. 2; it outputs a positive pulse pck, which is supplied to a typical latch shown on the right. PV_{dd} and pck waveforms obtained from HSPICE simulation are shown in Fig. 3 together with the waveforms at two internal nodes of generator, n_1 and n_2 .

Before PV_{dd} pulse arrives, M_1 is turned on and charges C at n_1 ; this turns on M_3 , so n_2 , which is disconnected from n_1 , is at 0 voltage. As PV_{dd} drops at the falling edge of pulse, M_2 is turned on, which allows the charges of C to be shared between n_1 and n_2 , i.e. n_1 voltage drops and n_2 voltage rises as shown in Fig. 3. Transistors M_1 and M_3 are made smaller than M_2 , so that main charge transfer occurs through M_2 in this process, when M_1 and M_3 are weakly turned on (note that the voltages of PV_{dd} and n_1 are decreasing). At the rising edge of pulse, M_2 is turned off and disconnects n_1 and n_2 ; C is slowly charged again through M_1 , which gradually turns on

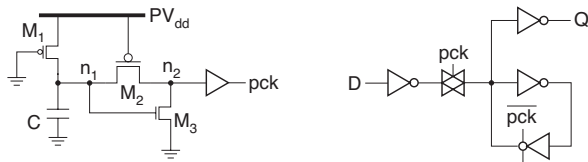


Fig. 2. A pulse generator and latch.

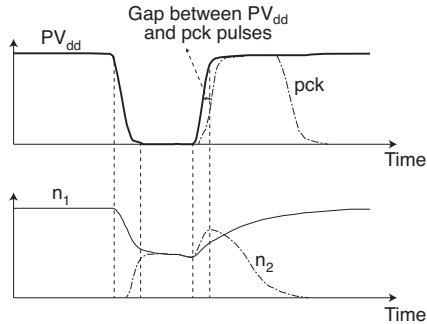


Fig. 3. Waveform of PV_{dd} and pck; n_1 and n_2 are internal nodes of generator.

M_3 . A pck pulse is regenerated from n_2 waveform by a buffer attached at the output of generator.

IV. EXPERIMENTS

A. Generator Design

The integrated generator and latch was designed in 32-nm technology. Its layout is shown in Fig. 4; it occupies 27% more area than D flip-flop, but if generator is made external and is shared by two latches, the area sum is estimated to be smaller than that of two flip-flops by 7%.

Post-layout HSPICE simulation indicates that pck pulse is 60.6 ps wide, which is wide enough for input data to be safely captured; pck pulse width in turn requires PV_{dd} pulse at least 53.6 ps wide with rise time of 8.6 ps and fall time of 10.0 ps. The gap between rising edge of PV_{dd} pulse and that of pck (see Fig. 3) was 9.2 ps; this is larger than 6.4 ps of setup constraint of latch, so latch input can be captured as soon as pck pulse rises as we have addressed in Section II.

B. Test Circuit Design and Assessment

A test design that performs USB function was selected from OpenCores [5]. Its RTL code was synthesized to yield 5676 gates and 1729 flip-flops; the layout was generated which contains clock tree; the implementation shall be called flip-flop circuit. Each flip-flop was then replaced by the integrated generator and latch shown in Fig. 4; the clock tree was removed and periodic PV_{dd} pulses were applied at one corner of V_{dd} network; a new implementation shall be named pulsed- V_{dd} circuit.

To verify whether pulsed- V_{dd} circuit functions correctly, the input and output waveforms of arbitrarily picked latch were obtained through HSPICE simulation as shown in Fig. 5(a). Corresponding waveforms of flip-flop circuit are illustrated in Fig. 5(b), which functionally match the waveforms of (a).

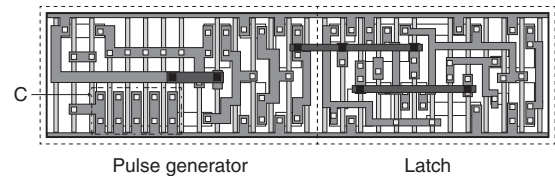


Fig. 4. Layout of integrated generator and latch.

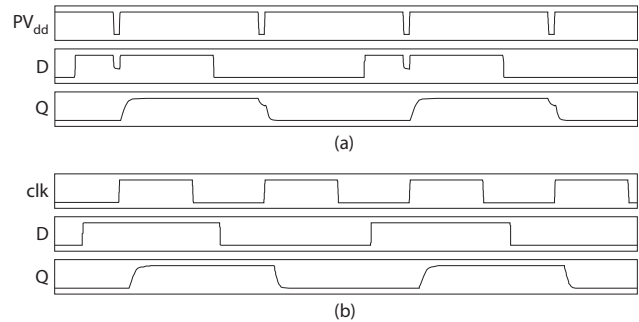


Fig. 5. Verifying functionality of (a) pulsed- V_{dd} circuit as compared to (b) flip-flop circuit.

Clock skew of pulsed- V_{dd} circuit was 5.7 ps. The small skew value is another benefit of pulsed- V_{dd} circuit; it is an understandable consequence because pulses are delivered over V_{dd} network, which has smaller RC delay. For fair comparison, an effort was put to achieve smaller skew for flip-flop circuit. The resulting clock tree contains 59 buffers and causes 11% larger total wirelength than pulsed- V_{dd} circuit; Monte Carlo simulation (to account for on-chip process variations on clock tree [2]) of the tree reported 22.3 ps of skew.

V. SUMMARY

We have argued that clock network can be dropped from synchronous circuit. Instead, V_{dd} network is made to carry periodic pulses, so it is now responsible for synchronization as well as usual power supply. A pulsed latch is employed as a sequencing element; a pulse generator, which is a key component, has been proposed.

A great deal of work are left to develop the proposed concept. Consistent supply of pulses over V_{dd} network is the foremost issue to be investigated. Existence of pulse on power supply implies a potential of charge recycling, which we will study for lower power consumption. A single pulse generator may be shared by more than one latch for the benefit of area.

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