Lithographic Defect Aware Placement Using Compact Standard Cells Without Inter-Cell Margin

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***Abstract*— Conventional standard cells contain extra space, called inter-cell margin, to prevent potential defects caused by lithography process. Margin is indeed necessary between some cell pairs, but there are also lots of cell pairs that do not yield any defects (or have very low probability of defects) when they are placed without margin. We address a new placement problem using standard cells without inter-cell margin. Placement should be done such that defect probability is made as small as possible while standard objectives such as wirelength is also pursued. The key in this approach is efficient computation of defect probabilities of all cell pairs and arranging them as a table that is referred to by a placer. We study how the cell pairs can be grouped by examining similar patterns along cell boundary, which greatly reduces the number of defect probability computation. The proposed placement method was evaluated on a few test circuits using 28-nm technology. Chip area was reduced by 10.8% on average with average and maximum defect probability kept below 0.4% and 4.1%, respectively.**

I. Introduction

Any kind of pattern failure, e.g. contact bridge and metal short, originated from lithography process is called lithographic defect. It has been become more important as patterns are scaled down to nano-meter geometry but lithography process does not fully support that fine feature.

A modern standard cell is designed in such a way that lithographic defect never arises within the region of a cell. This is done by repeated layout, retargeting and OPC, and verification through lithography simulation [1], [2]. Potential defects when cells are abutted together are avoided by reserving extra space, called inter-cell margin. Fig. 1(a) compares a cell before and after margin is added. A margin is typically the width of a single poly pitch and a dummy poly is inserted in the margin so that polys can be regularly placed for better lithography, as shown in Fig. 1(b).

Inter-cell margin, however, is not always necessary. In 28-nm technology we use in this paper, about 20% of cell pairs can be abutted together without margin but with zero defects, and about 30% of cell pairs with defect probability less than 10%. This suggests a possibility of new library consisting of compact cells without inter-cell margin. Some cells may be safely abutted for the benefit of reduction in area and wirelength; some others may be placed with extra whitespace in-between as shown in Fig. 1(c) if defect probability is expected to be high.

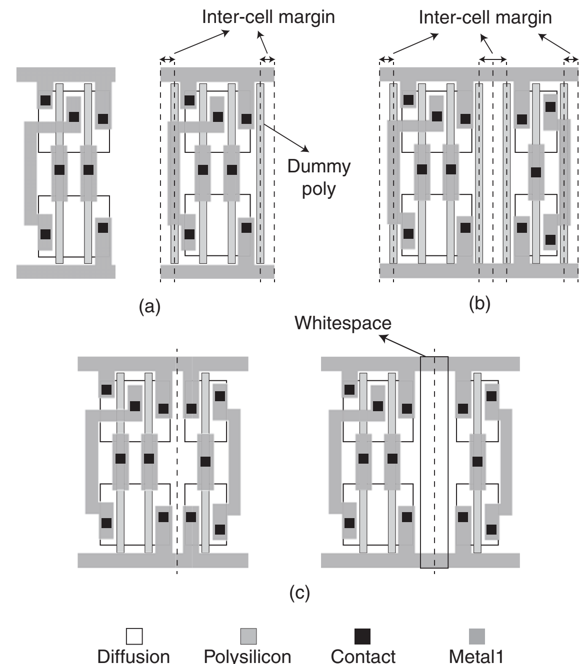

Fig. 1. (a) A cell without vs with inter-cell margin, (b) abutted cells with inter-cell margin, and (c) abutted cells without inter-cell margin vs abutment with extra whitespace in-between.

A. Contributions

We address a new placement problem, in which average (and maximum) defect probability is kept as low as possible; total wirelength, which is a popular objective, is also minimized. A key component in this problem is a table of defect probability. A challenge lies in probability computation time because it takes more than a minute for one cell pair and a practical library has a million number of cell pairs. This is addressed by two approaches: we experimentally show that the computation can be confined within 2-pitch range from cell boundary with tolerable error; the range of 2-pitch, called extent, can be classified into a few groups by identifying geometrically similar extents, which effectively reduces the number of cell pairs in great amount.

The remainder of this paper is organized as follows. Defect probability is defined in Section II, which also studies how probability computation can be approximated. Section III

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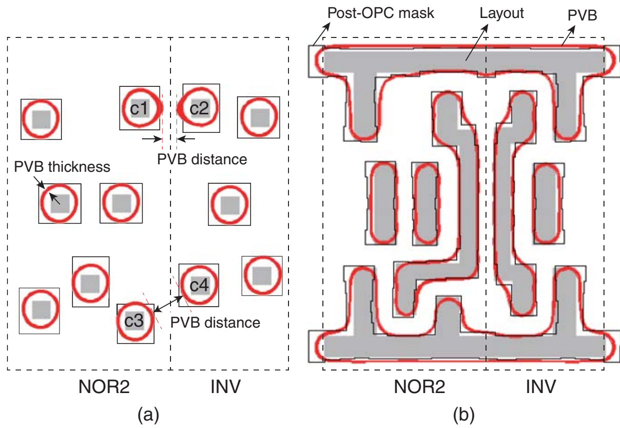

Fig. 2. PVBs in (a) contact layer and (b) metal 1 layer of two abutted cells.

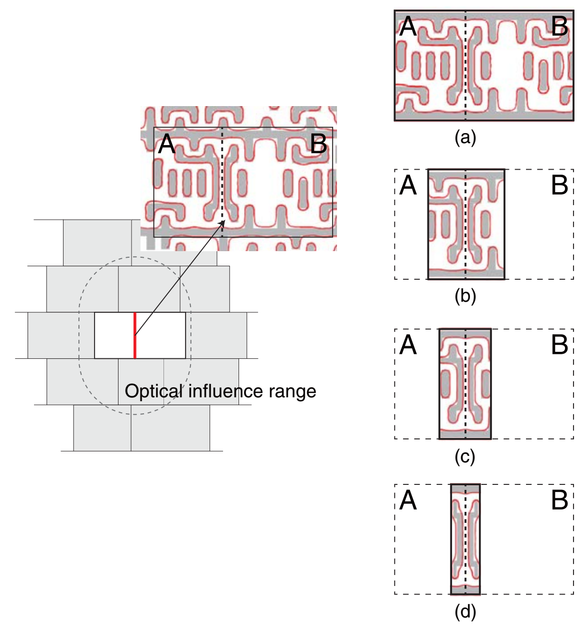

Fig. 3. Different settings for defect probability computation; lithography simulation in (a) full cell width, (b) within 3-pitch from boundary, (c) within 2-pitch from boundary, and (d) within 1-pitch from boundary.

addresses extent grouping. A prototype placement tool is described in Section IV, together with its experimental assessment. We draw conclusions in Section V.

II. Defect Probability Computation

A. Defect Probability

A pattern failure or defect caused by lithography process is usually modeled by using process variation band (PVB) [1], [3]. Fig. 2(a) illustrates PVBs of contacts in two abutted cells; PVBs of metal 1 layer is shown in Fig. 2(b). PVBs are obtained, after retargeting and OPC are applied to layout, by repeated lithography simulation at various lithography settings, which are combinations of extreme (and nominal) conditions of scanner focus, exposure energy, and mask error [3]. Thus, a PVB of each contact (or metal 1) is made of multiple contours, in which one contour corresponds to an exposed image on a wafer in particular lithography setting [1].

Note that contacts c1 and c2 are relatively close. Their PVBs along cell boundary look thicker, which implies more variation in the exposed image. This is due to the increased light interference as the two contacts are located closer. PVBs of c3 and c4, on the other hand, are thinner.

The probability that lithographic defect occurs, which we call defect probability, can be modeled by the minimum distance between PVB pairs, called PVB distance. Conventional cell is designed in a way that PVB distance within a cell is kept large enough so that defect never arises; it also includes inter-cell margin on both sides, which guarantees no defect when it is abutted to arbitrary cells. In our approach, we aim to remove all inter-cell margin, so some cell pairs may have non-zero defect probability. The defect probability when cells i and j are abutted together is modeled in a linear fashion and is given by

$$D(i,j) = \frac{M_{\rm pvb} - PD(i,j)}{M_{\rm pvb} - m_{\rm pvb}} \times 100\%, \qquad (1)$$

where $M_{\rm pvb}$ is PVB distance beyond which defect probability is 0%, $m_{\rm pvb}$ is PVB distance below which defect occurs in 100%, and $PD(i,j)$[1] is PVB distance between i and j. The values of $M_{\rm pvb}$ and $m_{\rm pvb}$ are typically available from foundry fab [3], [4]. Contact and metal 1 layers are the most critical layers for lithographic defect, so we measure $D(i,j)$ on two layers and consider the larger one as its value.

TABLE I
Maximum error of defect probability in different settings of lithography simulation

Layer	Maximum error of defect probability (%)			
	Full cell width	3-pitch from boundary	2-pitch from boundary	1-pitch from boundary
Contact	1.0	2.3	4.3	15.7
Metal1	1.0	3.7	5.3	37.0

B. Approximate Computation of Defect Probability

We assume 193nm ArF as an illumination source with immersion lithography in this paper. Optical influence range in this setting is about 1 μm, which reaches a few cells beyond cells A and B as shown in Fig. 3, whose defect probability we want to compute. Lithography simulation, which is performed at two layers and is repeated at various lithography settings as we discussed in Section II-A, turns out to take more than a minute. This is prohibitive because there are a million cell pairs for defect probability computation if a library contains 1000 cells.

Considering only abutted cells as shown in Fig. 3(a) fortunately yields negligible amount of error in defect probabil-

[1] $PD(i,j)$ and thus $D(i,j)$, in fact, have four different values because cells can be flipped along y-axis and the two cells can be abutted in two different orders.

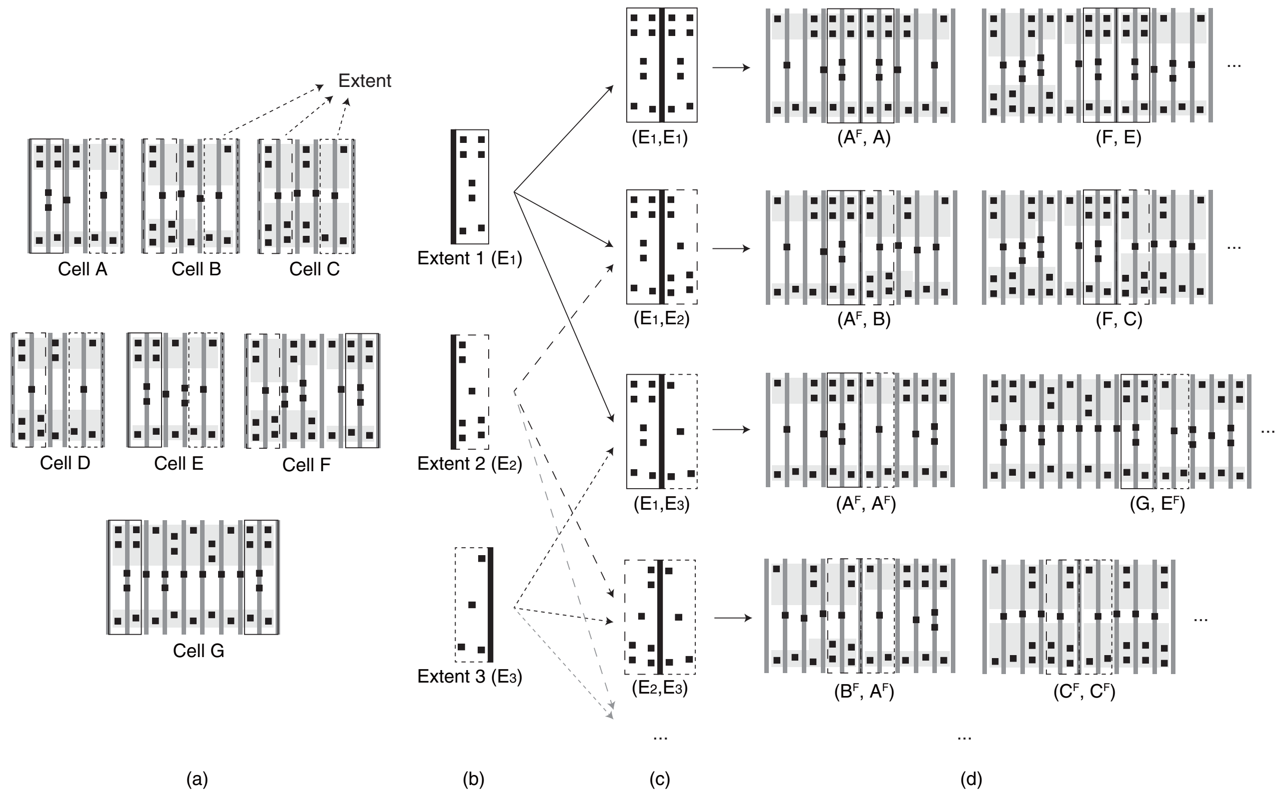

Fig. 4. (a) Library cells and their extents, (b) extent grouping, (c) extent abutment, and (d) mapping to cell abutment.

ity [5], [6]. The second column of Table I reports maximum error of defect probability for 1000 cell pairs, in which lithography simulation within full optical influence range serves as a reference; errors are 1% in both layers. We further decrease the range of defect probability computation to 3-pitch (3 times of minimum pitch of each layer) from cell boundary as shown in Fig. 3(b), 2-pitch in Fig. 3(c), and 1-pitch in Fig. 3(d), and assess the maximum error. As shown in Table I, 2-pitch from boundary seems to be a reasonable choice, which we assume for fast computation of defect probability in this paper.

III. Generation of Defect Probability Table

Even though we limit defect probability computation within 2-pitch range from cell boundary, a huge number of cell pairs still makes the computation intractable. We approach the problem by identifying the patterns along cell boundary and grouping them.

A. Extent Grouping

Fig. 4 illustrates the process. Let a library contain 7 cells. Contact patterns within 2-pitch range from cell boundary, called extents, are identified as shown in Fig. 4(a). They are compared and the same patterns are grouped as shown in Fig. 4(b). We then figure out how extents can be abutted as shown in Fig. 4(c). Note that extent, by its definition, can be abutted only along one side, which is denoted by thick line. Therefore, if there are n extent groups, there are $\left(\binom{n}{2}\right) = \frac{n(n+1)}{2}$ different ways extents can be abutted, which now serves as the number of defect probability computation; this is usually much smaller than the number of ways cells can be abutted (see Fig. 4(a)), $(2N)^2$, where N is the number of cells and $N > n$. Finally, cell pairs are mapped to corresponding extent pairs as shown in Fig. 4(d), in which $\mathrm{A^F}$ indicates the cell A with its orientation along y-axis flipped.

Our 28-nm library consists of 1043 cells thus 2086 extents. They are grouped into 944 in contact layer, and 1117 in metal 1 layer. Defect probability computation in this case is expected to take 198.0 and 346.6 hours, respectively, which are much less than 967.0 and 1208.7 hours when defect probability is computed for all cell pairs without any extent grouping.

B. Further Extent Grouping by Pattern Similarity Check

Defect probability computation still takes too much of time even after extent grouping. We try to reduce the number of extent groups by grouping similar (as well as exact) patterns together. We have tried three different criterion of similarity, 90%, 80%, and 70%. In 90% of similarity, for example, two extents are grouped together if more than 90% area is filled with 0 once we form geometric XOR of the extents.

The result of this new grouping is presented in Table II; the method of 100% similarity corresponds to the method of Section III-A. The number of extent groups is greatly reduced if we choose 90% as similarity criterion, e.g. from 944 to 388 in contact layer. The reduction in computation time of defect probability is roughly proportional to the square of

TABLE II
VARIOUS EXTENT GROUPING METHODS

Grouping method		# Extent groups	Defect probability computation	
			Time (hours)	Max error (%)
Contact	Similarity (100%)	944	198.0	5.7
	(90%)	388	18.6	6.6
	(80%)	236	5.3	19.7
	(70%)	116	1.6	34.1
Metal 1	Similarity (100%)	1117	346.6	4.8
	(90%)	416	23.7	6.1
	(80%)	299	19.9	24.7
	(70%)	185	2.3	36.2

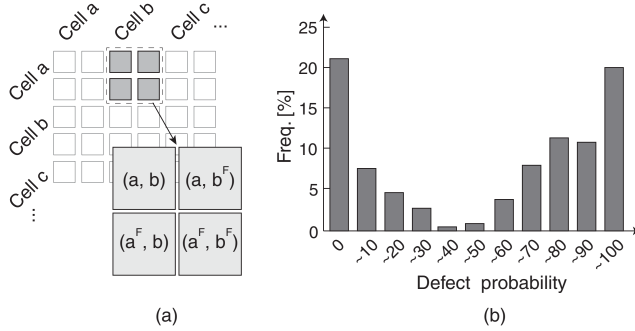

Fig. 5. (a) Defect probability table, and (b) defect probability histogram.

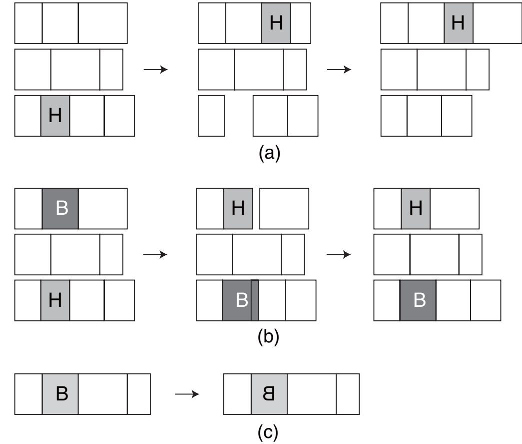

Fig. 6. Operations to generate a new placement.

the reduction in extent groups, which explains even greater reduction of time from 198.0 to 18.6 hours. Fortunately maximum error increases only marginally, from 5.7% to 6.6%. In similarity criterion of 80% and 70%, maximum error is now substantial, even though the number of extent groups and time for defect probability computation are further reduced. This is because a single extent group usually originates from a similar gate family (e.g. INV1X, INV2X, etc) in 90% similarity, while more than one gate family may constitute a single extent group in 80% and 70% similarity. We thus choose 90% similarity in our defect probability computation.

Fig. 5(a) pictorially shows defect probability table, which has 2086 rows and 2086 columns. Fig. 5(b) summarizes defect probabilities as a histogram; it indicates that defect probability is widely distributed, which should be carefully taken into account when cells are placed.

IV. Defect Probability Aware Placement

As shown in Fig. 5(b), many cell pairs have non-negligible defect probability when they are abutted. This fact lends itself to automatic placement problem, in which average (and maximum) defect probability is kept as low as possible; other usual objectives such as wirelength should also be taken into account. A prototype tool has been developed based on simulated annealing to solve the problem [7], [8].

A. Cost Function

Each placement during simulated annealing is evaluated by using a cost function:

$$\Gamma = \alpha C_w + \beta C_r + \gamma C_d, \tag{2}$$

where C_w is total wirelength measured by using half-perimeter of bounding box. C_r is introduced to reserve enough amount of whitespace in each circuit row, so that cell pairs with larger defect probability can be separated apart; it is given by

$$C_r = \sum_{\forall \text{row } i} \left(WS_{req}(i) + RL(i) - RL_0 \right)^2, \tag{3}$$

where $WS_{req}(i)$ is the whitespace that is required to have defect probability of all cell pairs in row i below some threshold (which is a parameter to control the maximum defect probability), $RL(i)$ denotes the sum cell width of row i, and RL_0 is the minimum $RL(i)$ in the initial placement. C_d corresponds to the average defect probability of all cell pairs.

Coefficients α, β, and γ are employed to balance the quantity of the three terms. Since C_w and C_r tend to increase with the number of cells while C_d does not, we empirically set α and β to 1 and γ to the number of cells divided by 100.

B. Implementation of Placement

The input to our placement tool includes a target aspect ratio of placement region and the amount of whitespace as

TABLE III
COMPARISON OF THREE PLACEMENT METHODS

Circuit			Standard placement with conventional cells (A)		Standard placement with compact cells (B)			Proposed placement with compact cells (C)			
Name	# Cells	# Nets	C_w (mm)	Area (um^2)	C_w (%)	C_d	Area (%)	C_w (%)	C_d	Max defect prob	Area (%)
sasc	349	365	2	551	93.3	71.2	90.3	101.7	0.9	4.2	90.3
i2c	515	550	3	682	91.9	66.1	88.9	100.2	0.4	4.1	88.9
spi	1249	1330	10	1637	99.0	66.3	88.8	98.3	0.3	4.2	88.8
wb_dma	2160	2423	21	2728	92.2	67.5	88.5	93.8	0.4	4.1	88.5
tv80	3932	3980	44	4356	94.8	64.9	86.8	96.8	0.2	4.2	86.8
mem_ctrl	4511	4663	56	5937	95.0	44.0	88.9	101.7	0.3	4.1	88.9
ac97	6310	6382	104	10299	90.5	66.6	91.0	97.6	0.5	4.1	91.0
usbf	7492	7991	132	9452	93.2	59.8	88.5	98.2	0.4	4.0	88.5
pci	9996	10297	247	16664	91.8	63.4	91.2	93.7	0.5	4.1	91.2
aes_cipher	11112	11371	152	9974	91.3	80.9	83.8	97.1	0.2	4.0	83.8
ethernet	31034	31286	469	54756	92.0	70.6	91.7	98.1	0.4	4.0	91.7
vga_lcd	46203	46339	990	86162	93.5	69.6	92.2	97.2	0.3	3.9	92.2
Average			–	–	93.2	65.9	89.2	97.3	0.4	4.1	89.2

percentage of that region. The number of circuit rows is then identified from the input and the sum area of all cells that will be placed.

The placement consists of two steps: repeated placement using simulated annealing and whitespace distribution to further reduce defect probability. Three operations are performed to generate a new placement for the first step. The first operation shown in Fig. 6(a) displaces a randomly picked cell (cell H) to a randomly chosen place; cell overlap and inter-cell whitespace are removed accordingly. The second operation shown in Fig. 6(b) switches the location of randomly picked cell pairs (B and H). In the final operation shown in Fig. 6(c), a cell (B) is picked, and its orientation along y-axis is flipped. The operations are applied with different probability, which is heuristically determined.

While the three operations are applied to generate a new placement, whitespace is allowed only at the right end of each circuit row. The second step of placement starts once the simulated annealing completes, and distributes whitespace so that defect probability can further be reduced. All cell pairs with the defect probability being larger than some threshold (the same threshold to control C_r) become the candidates, and whitespace of 1-poly pitch (to keep pitch regularity of polysilicon for stable patterning result [9]) is distributed in greedy fashion.

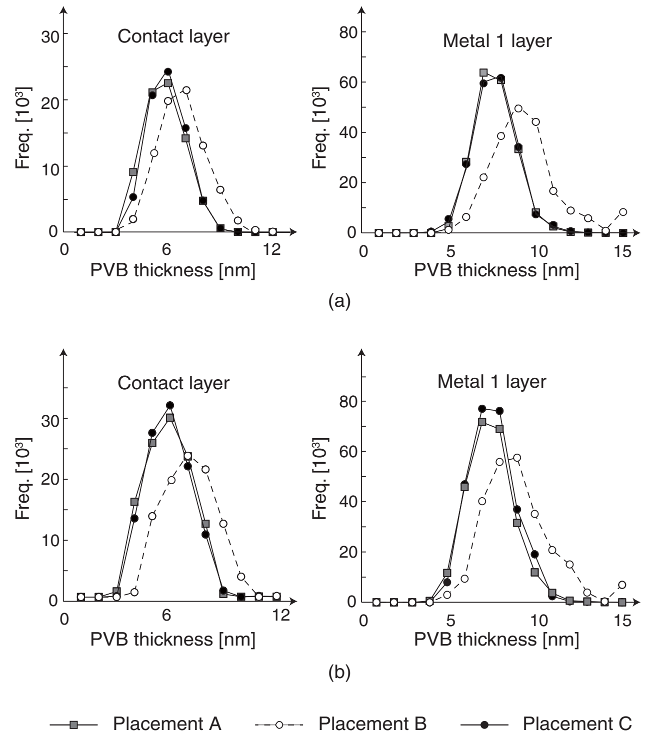

Fig. 7. Histogram of PVB thickness of contact and metal 1 layer: (a) mem_ctrl and (b) ac97.

C. Experimental Results

The proposed placement method was evaluated using 12 test circuits from open cores [10]; circuit information is listed in the first three columns of Table III. A square placement region was assumed and 20% of total region was dedicated to whitespace. The experiment was based on commercial 28-nm technology.

Three placement methods were implemented and compared. The first method (placement A) is a standard placement, which places conventional cells having inter-cell margin and minimizes total wirelength; in this method, γ is set to 0 in (2) and $WS_{req}(i)$ is dropped from (3). Resulting C_w and chip area are reported in columns 4–5; defect probability is always 0 thanks to inter-cell margin. The second method (placement B) is the same as placement A but cells are now without inter-cell margin. Area is shown in percentage of the area from placement A; it is reduced by 10.8% on average, which is the main advantage of deploying cells without inter-cell margin. Total wirelength, which is also shown in percentage number, is reduced too as a result of reduced chip area; but, defect probability is necessarily very high.

The proposed method is named placement C. It achieves the same area reduction as placement B. But, average defect

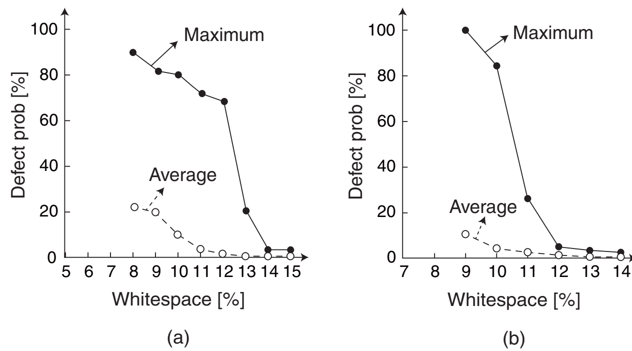

Fig. 8. Defect probability with varying whitespace: (a) spi and (b) sasc.

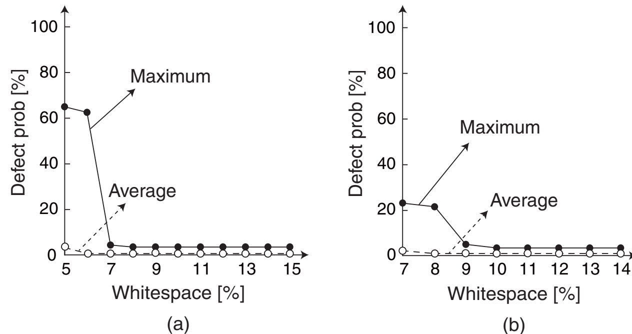

Fig. 9. Defect probability when circuits are synthesized using defect–friendly cells: (a) spi and (b) sasc.

probability C_d is kept very low, less than 1% in all test circuits. This comes at the cost of increase in the total wirelength if C_w from placement B and C is compared. We also report maximum defect probability from placement C; it is affected by the threshold used to control the quantity of (3) and to perform whitespace distribution; we set that value to 5.0%, which was honored by all test circuits. PVB thickness is also the measure of lithographic defect [11], so we extracted its distribution as a histogram from three placement methods and compared. As shown in Fig. 7 placement C achieves almost identical histogram as placement A, which is understandable consequence of very low defect probability from placement C.

The amount of whitespace clearly affects average and maximum defect probability from our placement method. We repeated the placement while we vary whitespace percentage for a few test circuits. The result for two sample circuits is shown in Fig. 8; 15% whitespace, which represents very tight placement [12], was the point beyond which maximum defect probability is kept below 5%.

Fig. 5(b) indicates that there are many good cells in terms of defect probability but there are also many bad cells. We may try to avoid those bad cells right from logic synthesis, which will make placement easier. We excluded cells whose average defect probability (over all cell pair combinations that include those cells) exceeds 50% from a library; 617 out of 1043 cells fell in that category, in which AND2X and BUF11X were examples. We took the same circuits of Fig. 8, re–performed logic synthesis, and repeated the same experiment of Fig. 8. The result is shown in Fig. 9. Both average and maximum defect probability can now be kept low using smaller amount of whitespace, which can be expected. This comes at the cost of increased circuit area due to less freedom of logic synthesis; sum of cell area increases from 1277 to 1459 in spi and from 574 to 609 in sasc.

V. Conclusion

Conventional standard cells contain inter-cell margin to prevent potential lithographic defects. We advocate that the margin can be removed for the benefit of chip area and wirelength, while defect probability is affected very little when cells are carefully places. A prototype placement tool has been developed and experiments have been performed to prove our argument.

A key component in this approach is the table of defect probability of all cell pairs, which placement refers to for calculating its cost function. A straightforward computation of defect probability is intractable because of large lithography simulation time and large number of cell pairs. We have shown that the computation can be confined within 2-pitch range from cell boundary with tolerance amount of error; the range of 2-pitch, called extent, has been shown to be classified into a few groups by grouping geometrically similar extents, which greatly reduces the number of computation.

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