Calibration of Interconnect Corners Using On-Chip Ring Oscillators

Daijoon Hyun‡§ and Youngsoo Shin§

‡ Samsung Electronics, Hwasung 445-330, Korea
§ Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea

***Abstract*— Interconnect corners should accurately reflect actual interconnect in silicon to ensure proper design signoff. On-chip ring oscillator (ROSC) based calibration of interconnect corners is proposed. It comprises extraction of ROSC delay as a function of interconnect resistance and capacitance, projection of measured delay on that function, and identifying how existing corners should be adjusted. Simulation using a new calibrated corner demonstrates an excellent match with measurement in 14-nm test chips.**

I. Introduction

Manufacturing variations are characterized by device- and interconnect-corners [1]. Device corners are represented by the performance of nMOS and pMOS devices, e.g. FF when both devices are fast. Interconnect corners correspond to combinations of extreme resistance (R) and capacitance (C) values [2], [3] as illustrated in Fig. 1. As an example, C_{min} is a corner in which the metal wire is patterned with larger width and thickness so C becomes smaller and R becomes larger; if, in addition, the height of ILD (inter layer dielectric) becomes smaller, C slightly increases with the same R, which yields RC_{max} corner where RC product is maximized.

Designers rely on interconnect corners for signoff, so it is important to ensure that real interconnect in silicon matches one of corners or at least falls within the shaded region spanned by corners. A usual practice for this purpose is to prepare a few metal patterns in scribe lines, measure R and C from sample test dies, and adjust corners accordingly. This however is not ideal because interconnect parasitics are strongly affected by actual metal patterns, particularly in copper damascene process these days.

We use on-chip ring oscillators as a means of calibrating interconnect corners. A ring oscillator is first simulated using existing corners; its delay is then formulated as a function of interconnect resistance and capacitance; actual delay from silicon is then projected on that function, which yields candidate corners for calibration; the process is performed for a few variety of ring oscillators so that various interconnect structures can be accounted for in calibrated corners.

II. Interconnect Corner Calibration

Assume a ring oscillator of certain configuration. Its delay is simulated using SPICE in each of interconnect corners shown in Fig. 1. The resulting delay values are located in the space of R and C with z-axis as a delay as illustrated in Fig. 2. We

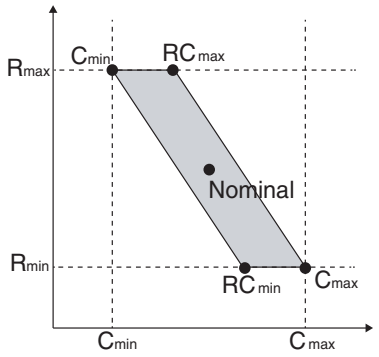

Fig. 1. Interconnect corners.

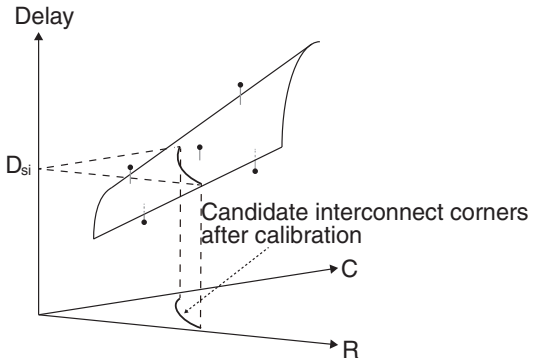

Fig. 2. Interconnect corner calibration: extracting surface of delay D from simulated delay values, and identifying (R, C) values on the surface corresponding to measured delay D_{si}.

regard the ring oscillator delay as a function of R and C, and want to derive a curved surface that passes all 5 points. Let the delay be given by

$$D = k_1 R + k_2 C + k_3 RC + k_4. \quad (1)$$

Since there are 5 delay points with 4 unknown coefficients, we derive curved surface that are close to all points as much as possible instead of the surface that passes all of them. This is achieved by minimizing the sum of squared error between (1) and actual simulated delay. The resulting curved surface is illustrated in Fig. 2. We now locate the ring oscillator delay from silicon measurement, denoted by D_{si}, and try to identify which R and C values on the curved surface that delay

TABLE I

INTERCONNECT LENGTH AND WIDTH OF DIFFERENT ROSC TYPES

ROSC type	Length	Width
I	1×	1×
II	10×	1×
III	10×	2×
IV	30×	1×

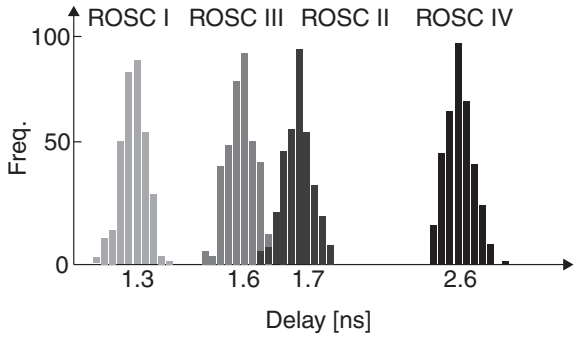

Fig. 3. Measured delay distribution of ring oscillators.

corresponds to; those values typically form a curve as shown in Fig. 2. Note that device delay should match in this process, i.e. it should be guaranteed that devices are in the same process corner both in simulation and silicon measurement.

We prepare 4 different types of ring oscillator as listed in Table I to account for various interconnect structures. They differ only in the length and width of interconnect used. For each of ring oscillator, we apply the aforementioned procedure and obtain the curve on R-C space. There are 4 curves now which are unlikely to intersect at a single point, but we want to identify a single R and C value, denoted by (R_{si}, C_{si}), which will correspond to final calibrated corner. We thus perform least squares, i.e. minimize the sum of squared error between measured delay D_{si} and estimated delay (1) with R and C being set to unknown R_{si} and C_{si}, respectively.

The final interconnect corner (R_{si}, C_{si}) is now prepared in standard technology format [5] and is offered to designers.

III. EXPERIMENTS

A test chip is designed in 14-nm commercial technology; it contains 4 ring oscillators listed in Table I. About 350 dies are sampled and ring oscillator delays are measured. The distribution of delay for each ring oscillator type is shown in Fig. 3. The median value of each distribution, which is identified in x-axis, is considered as a representative delay and corresponds to D_{si}. This approximation is acceptable since delays are very narrowly distributed, e.g. sigma in ROSC I is 12ps, which is less than 1% of median value. The calibrated interconnect corner following our method is (C_{si}, R_{si}) = (1.20, 0.60) if each value is normalized to corresponding value at nominal corner; it is near C_{max} corner in which (C_{max}, R_{min}) = (1.17, 0.78), but is clearly outside of shaded region spanned by existing corners (see Fig. 1) indicating the importance of silicon-based corner calibration.

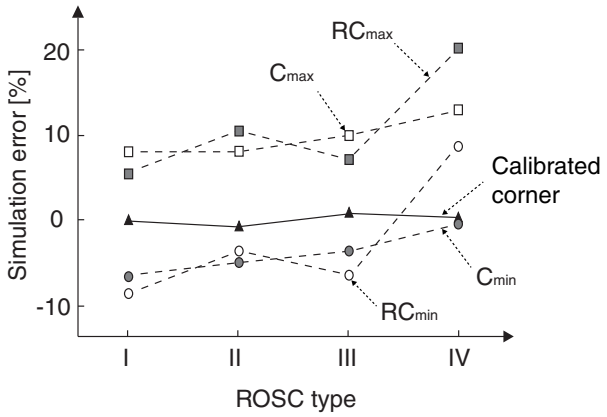

Fig. 4. Simulation error of ring oscillator delay (with measurement as a reference) with calibrated- and existing-corners.

The calibrated corner is used to simulate the ring oscillators using SPICE again. The accuracy of simulated delay, with measured delay from Fig. 3 as a reference, is presented in Fig. 4. Unsurprisingly, the simulation matches measurement very well. Metal patterns were also prepared in scribe lines, and their parasitics were measured; C and R values are (1.15, 0.90), which is some distance away from (C_{si}, R_{si}); this demonstrates inaccuracy involved in using scribe line patterns as a way of calibration.

As a comparison, the simulation error with existing corners is also presented. The errors tend to increase as the wire gets longer (if ROSC I, II, and IV are compared). This comes from the mismatch of R and C between the simulation and the measurement, and the error increases as the wire delay takes larger proportion. Errors are more diverse as interconnect becomes longer (e.g. if ROSC I and IV are compared), which implies the need for an additional timing margin in long global interconnect.

IV. SUMMARY

An on-chip ROSC based calibration of interconnect corners has been proposed and demonstrated using 14-nm test chips. It has also been shown that a usual practice of using scribe line patterns for corner calibration is inaccurate and is not an appropriate solution. The method should be validated in real product designs, which remains our further work.

REFERENCES

[1] D. S. Boning and S. Nassif, "Models of process variations in device and interconnect," in *Design of High Performance Microprocessor Circuits, chapter 6*. IEEE Press, 2000, pp. 98–115.

[2] K. Yamada and N. Oda, "Statistical corner conditions of interconnect delay (corner LPE specifications)," in *Proc. Asia and South Pacific Design Automation Conf.*, Jan 2006, pp. 706–711.

[3] F. Huebbers, A. Dasdan, and Y. Ismail, "Multi-layer interconnect performance corners for variation-aware timing analysis," in *Proc. Int. Conf. on Computer-Aided Design*, Nov 2007, pp. 713–718.

[4] N. S. Nagaraj, T. Bonifield, A. Singh, and C. Bittleestone, "BEOL variability and impact on RC extraction," in *Proc. Design Automation Conf.*, Jun 2005, pp. 758–759.

[5] *StarRC User Guide*, Synopsys, Mountain View, CA, Dec. 2014.